Radio Shack®

Service Manual

26-1125

TRS-80®

Model III Computer Graphics Upgrade Kit

Catalog Number 26-1125

CUSTOM MANUFACTURED IN U.S.A. BY RADIO SHACK, A DIVISION OF TANDY CORPORATION

Contents

Illustrations

1/ Introduction

The Model III Hi-Res Graphics Board is an internal upgrade for the TRS-8Ø Model III Microcomputer that provides bit graphics with a resolution of 64Ø horizontal dots by 24Ø vertical dots. The Graphics Board is port mapped, and based on the MC6845 CRTC chip. Either normal Model III video or graphics may be displayed at any one time, but not together. Screen locations are accessed in an "X - Y" format, with options provided for automatic incrementing or decrementing the horizontal or vertical address registers.

2/ Specifications

* High resolution graphics display generator designed for installation inside the Model III Case.
* 64Ø x 24Ø bit addressable dots.
* Port mapped addressing with auto-increment and auto-decrement capability.
* 32,768 bytes of user memory organized as an X-Y matrix of 128 x 256.
* 78.9 ns dot spacing.
* 15,84Ø Hertz horizontal frequency.
* 6Ø or 49.97 Hertz vertical frequency.
* Operates on +5 volts at Ø.6 Amps.

3/ Theory of Operation

Note: Refer to the Block Diagram for the following:

The Processor interfaces to the Graphics Board through the address and data buffers. Addresses are sent to the Address Decoding block where signals are generated to activate various sections of the Graphics Board. The data buffer is bi-directional, and buffered data lines are connected to the Cathode Ray Tube Controller (CRTC) the Options Register, the X and Y Counters, the Nybble Write Multiplexer and the Byte Read Latch. Signals from the Address Decoder/Device Selection block as well as from the Options Register are sent to the CPU Handshake block where other processor interface signals, such as WAIT*, are produced.

All timing for the Graphics Board is referenced to the 12 MHz crystal oscillator. The output from this oscillator is fed to a divider network that produces the necessary signals to interface to the Dynamic RAMs (DRAMs). The raw clock signal is also used as a shift clock to shift the graphics bits out of the Shift Register. Another signal produced by the divider is CRTCLK, which is used to clock the CRTC. This chip produces the necessary synchronizing and blanking pulses required by the video monitor, as well as the screen refresh addresses required by the DRAM.

The display DRAM addresses generated by the CRTC are sent to a ROM section which translates the addresses into an X,Y format. This is necessary to make the addresses (from the CRTC) agree with the addresses programmed into the X and Y Counters, so that the correct screen location is accessed. (The X,Y format greatly simplifies the writing of software.)

Both sets of addresses (those from the CRTC and those from the X,Y Counters) are sent to a four-to-one multiplexer, which selects the appropriate addresses to be sent to the DRAM. When the CPU is accessing the DRAM, the addresses come from the X,Y Counters. When the screen is being refreshed or updated, the addresses come from the CRTC by way of the ROM translator. The two signals that decide which of the four address inputs is conveyed to the output, come from the CPU Handshake Logic block (which selects whether the addresses come from the X,Y Counters) and the Timing block (which selects whether the addresses are X addresses [row addresses] or Y addresses [column addresses]). The appropriate addresses arrive at the DRAM array along with the signals RAS* and CAS* from the timing section.

During a Write cycle, the W* signal comes from the CPU Handshake Logic block, and the data to be written comes from the Nybble Write Multiplexer. If the cycle is a Read cycle, there is no W* signal, and the DRAM Q outputs are fed simultaneously to the Nybble Read Latch and the Shift Register. Note that the DRAMS are organized in a 64K x 4-bit array. Since the DRAM is in a 4-bit array, and the CPU communicates with 8-bit data, some provisions must be made to accomodate this difference. How this is accomplished will be discussed in a later section.

The Q outputs from the DRAM array are sent to the Shift Register, four bits at a time, where the bit information is clocked to become a video output signal. This video output signal, as well as the sync outputs of the CRTC, are sent to a video multiplexer, which selects either these signals or the normal video and sync outputs from the Model III, to be sent to the monitor. The signal that decides which signal is to be output from the multiplexer comes from the Options Register, and is called GRAPHICS/ALPHA*.

The Options Register also controls the additional signals necessary to load a value into the X,Y Counters, and programs the Counters to either remain stationary, or automatically increment or decrement either Counter.

Note: Refer to the Schematic Diagram for the remainder of the discussion of Theory of Operation.

Processor Interface

The Processor address lines AØ-A7 (excluding A2, which is not used on the Graphics Board) are buffered and inverted by hex inverters U25 and U28. A5* and A6* are ANDed by U22, pin 8 (74LSØ8) to produce the active high signal "ADR". This signal is used to reduce the redundancy of ports decoded by the address decoder. All other buffered address lines (AØ*, Al*, A3*, A4*, A7*) are now active low.

Incoming control signals XIN*, XOUT*, and XRESET* are buffered by additional sections of U22 and U25. The uncommitted inputs of U22 (pins 2 and 4) are pulled high by R4, a 4.7K pullup resistor. XIN* is inverted twice, to buffer it and keep it active low for the rest of the board. The active high state of this signal (after the first inverter) is NANDed with the signal GPSEL from the Address Decoding section to produce the active low signal EXTIOSEL*, which is used by the Model III to enable the data buffers for the port connector. An open collector gate, *U2l (7438) is used for this signal in order that other open collector signals may be "wire-ORed" to the same line without any damage to any of the devices that produce this signal. The WAIT signal from the CPU Handshake Logic section is also fed through another section of U2l for the same reason.

Address Decoding/Device Selection

Address Decoding and Device Selection is accomplished by part of the PAL (U8) and by the dual 1 of 4 decoder, U13 (74LS139). The logic equations for the PAL are shown in the lower left corner of Sheet 1 of the Schematic Diagram. The bottom four equations are involved in address decoding. The first of these four equations signifies that the signal GPSEL* will be low (active) when A7 is high, A4 is low, and ADR is high. Recalling that ADR will be high when A5 and A6 are both low, it is evident that this GPSEL* will be active any time a port in the address range from 8Ø Hex to 8F hex is accessed. As stated above, this signal is sent back to the Model III to enable the IO bus buffers.

The next PAL equation concerns the signal VSEL*, and states that this signal will be active when A7 is high, ADR is high, A4 is low, and A3 is high. This is the same as the above equation with the addition of the term, A3. Therefore, this signal will be low during any access from 88 Hex to 8F Hex. This signal is used to enable the CRTC. (AØ is also connected to the Register Select input to the CRTC.) The ports 88 and 89 Hex are therefore used to program the internal registers of the CRTC. Since A1 and A2 are not terms in this equation, the CRTC ports are dual addressed four times in the range of 88 through 8F Hex.

The two remaining address decoding signals generated by the PAL (U8) are called READ* and WRITE*. READ* is active during any IN cycle in the address range of 8Ø through 87 Hex. WRITE* is active during any OUT cycle in the same address range. These signals are sent to U13 (74LS139) for further decoding. The READ* signal is used to enable one-half of the dual 1 of 4 decoder, while the WRITE* signal is used to enable the other half. The two least significant address lines (AØ and A1) are then decoded into four READ signals and four WRITE signals. The following table shows which addresses correspond to what signals:

Port	R/W	Signal Name	Function
8Ø	Rd	OPTIONSRD*	(Not used)
81	Rd	VIDRAMRD*	CPU reads from Video RAM
82	Rd	YREGRD*	CPU reads from the Y Register
83	Rd	XREGRD*	CPU reads from the X Register
8Ø	Wr	OPTIONS*	CPU writes to Options Register
81	Wr	VIDRAM*	CPU writes to Video RAM
82	Wr	YREG*	CPU writes to the Y Register
83	Wr	XREG*	CPU writes to the X Register

These signals are dual addressed, and are mapped into the address range of 84 to 87 Hex also.

Data Handling

Data to and from the CPU is handled by the data buffer, U31, an 8-bit bidirectional buffer (74LS245). The buffer is enabled by GPSEL*, which, you'll recall, is active for any access in the range of 8Ø through 8F Hex. The direction of data transfer is determined by the signal IN*. The Graphics Board data bus from this buffer is connected to the CRTC, the X,Y registers (Counters), the Options Register, the Nybble Write Multiplexer, and the Byte Read Latch.

Whenever data is to be written into the Video RAM, it is impressed upon both halves of the Nybble Write Multiplexer. During the CPU Write cycle, a WAIT state is generated and a signal called XADR7 switches the Nybble Write Multiplexer outputs from one set of inputs to the other. Therefore, during any one CPU Write cycle, there are actually two RAM write cycles.

Similarly, whenever the CPU is to read data from the Video RAM, a WAIT state is generated to the CPU while two RAM Read cycles take place. During the first RAM Read cycle, the most significant nybble of data is latched into the Nybble Read Latch (U11) by a signal called STROBE*. During the second RAM Read cycle, this data, as well as the least significant nybble, is latched into the Byte Read Latch (U1Ø) by a signal called RDLATCH. U1Ø is a 74LS374, which has three-state outputs. These are then enabled by a signal called VIDRAMRD* (from the Address Decoding and Device Selection circuitry discussed above) and the data is gated onto the data bus. There will be a detailed discussion of the intricate timing that is necessaray to accomplish these double Read and Write cycles later on.

RAM Array

The RAM array consists of four 64K by 1 bit DRAMs. Since the dot resolution is 64Ø horizontal by 24Ø vertical, a total of 153,ØØØ bits are needed, which is well within the capability of our array (which is 256K). These DRAMs require only a single voltage supply (+5 volts). Due to the double Read and Write cycles, these DRAMs must be very fast, and are specified at a 15Ø nano-second access time.

Address Generation/CRTC

Two methods must be provided for addressing the Video RAM, one for the CPU so it can read or change the contents of the RAM, and one for the CRTC so it can extract the bit information to be displayed on the screen. The CPU addresses are provided by the X and Y Counters (U17, U18, U19, and U2Ø). These are Four-bit Synchronous Up/Down Counters that can be preloaded with any given count.

This preload function is used to latch the appropriate X and Y coordinates from the data bus with an XREGWR* or YREGWR* signal from the Address Decoding/Device Selection circuitry. Once a desired starting location has been latched into these 74LS191's, they can be made to count up or down by setting the appropriate bits in the Options Register and providing additional writes or reads to the Video RAM.

The addresses are provided in an X,Y format for the convenience of the programmer. Each X address defines eight horizontal dot positions on the screen, while each Y address defines one vertical dot position on the screen. For a given X address, each data bit defines one horizontal dot position. Therefore, since the horizontal resolution is 64Ø dots, a total of 8Ø x addresses (64Ø/8) are needed. This means that seven bits of the X Register are used. Since 24Ø Y addresses are needed, all eight bits of the Y register are used.

U2Ø is used to latch or count the least significant four bits of the X address, while U19 is used for the most significant three bits. Note that when these registers are used as a counter, the ripple carry output of U2Ø is connected to the clock in U19, so that each time U2Ø "wraps around", U19 is incremented. Therefore, these two units function as one seven bit counter. Similarly, U18 is used for the least significant four bits of the Y address and U17 is used for the most significant four bits. Again, they function as one eight bit counter.

For screen update and screen refresh (not to be confused with dynamic RAM refresh), the CRTC is used to generate the addresses. The CRTC inputs include eight data lines that are connected to the buffered data bus, a PGSEL (Program Select) line which is connected, along with RESET*, to the buffered system RESET* signal, E, RS, and CLK. The E line is used for read/write synchronization, and is therefore connected to the negative OR of IN* or OUT* from the Z8Ø. The RS line is the Register Select line and is connected to the true version of AØ. CS* is the chip select, and is driven by VSEL* from the address Decoding/Device Selection block.

The clock input to the CRTC is one-eighth the frequency of the dot clock, which is consistent with each X address defining eight dot positions. For each cycle of the CRTCLK, the addresses put out by the CRTC increment by one, until the maximum address has been generated (the page is full and vertical sync occurs).At this time they start over at ØØØØ.

Since the CRTC was originally designed for use with a charaacter generator, the addressing is slightly more complicated than that of a simple counter. As the horizontal dimension is set up for 8Ø (decimal) locations, the lower seven Memory Address lines (MAØ through MA6) count modulo 8Ø.

When the count is complete, the Row Addres lines (RAØ through RA3) increment by one until they reach the Maximum Row Address count that is programmed into the CRTC (in this case, 9). At this time, the remaining Memory Address lines (MA7 through MA1Ø) are incremented until the page isw complete.

The CRTC address generation has one additional problem that must be solved. Specifically, the addresses put out by the CRTC are segmented by the relationship between the MA lines and the RA lines. These do not correspond to the X,Y format produced by the X,Y Counter registers used for CPU update.

In order to make the CRTC addresses correspond to the X,Y registers, a pair of bipolar ROMs (U29 and U3Ø) is used. These take the non-linear addresses of the CRTC and translate them into the appropriate addresses to match the X,Y registers. Additionally, the Y registers are latched into an eight bit latch, U34 (74LS273). Since page mode access of the DRAMs will be employed (remember that there are two RAM cycles for each CPU cycle), we are essentially latching the Column Addresses for the DRAMs.

Address Multiplexing

Up to this point, we have four sets of addresses to be sent to the DRAMs: the CPU X and Y addresses and the CRTC X and Y addresses. Four dual one-of-four multiplexers (U23, U24, U26, and U27 [74LS153]) are used to select which set of addresses is passed to the DRAM array. These multiplexers have two select inputs. The binary pattern on the select inputs determines which of the four sets of two inputs is routed to the two outputs for each chip.

The "A" input of each chip is connected to the MUX signal from the timing section and selects between X (row) addresses and Y (column) addresses. The "B" input of each multiplexer is connected to a signal called VDCPU, and is used to select between CRTC-generated addresses and CPU-generated addresses. The only time the CPU-generated addresses are selected is during a horizontal or vertical retrace period.

System Timing

Note: For the purpose of this discussion, refer to the Timing Diagrams (Figures 4 and 5) as well as the Schematic Diagram (Figures 8 and 9).

All timing for the Model III Graphics Board is referenced to the 12.672 MHz clock. An oscillator is made up of two swamped inverters (U1, pins 8 and 1Ø), coupling capacitor C9, and crystal Y1. The oscillator is buffered by U1, pin 12 to provide the necessary current to drive other TTLs without loading the crystal. This clock signal is used to shift the bits out of the Shift Register, to clock the MUX flip-flop (U7), as an input for the PAL (U8), and the counter, U2 (74LS161).

U2 is a synchronous four bit counter. It is permanently enabled; the load and clear inputs are tied high; and the carry output is not used. As the most significant bit is not used, the chip functions as a divide-by-eight. Capacitors C3 and C41 are used to suppress unwanted harmonics and thus reduce RFI. The most significant output that is used is CRTCLK, which is one-eighth the frequency of the dot clock.

All outputs from the divider, as well as the CLK signal itself, are fed into the PAL(U8). The outputs we are concerned with are RAS*, CAS* STROBE, and XADR7*. The equations at the bottom left of the Schematic Diagram (Sheet 1) and the Memory Timing Chart (Figure 4), illustrate how these signals are produced. Note that the inputs QA, QB, and QC come from the divide-by-eight, and that each is a divide-by-two of the previous signal (QA is CLK divided by two). Also, the signal CRTCLK is the same as QC.

The RAS* signal is generated when QB is high and QC is low. This is shown on the Timing Diagram. The CAS* signal is a little more complicated - it is low when QB is high, or when QA is high and QB and QC are both low. This is necessary in order to get two CAS* cycles for each memory cycle, which is a requirement for page mode operation of the DRAMs.

The RAS* signal, in addition to controlling the Row Addresses for the DRAMs, is inverted and called LTCH*. This signal is used to latch the Column Addresses into U34 (74LS273). This insures that the DRAM array will get a consistent Column Address during both CAS* intervals of a double write cycle. Only the Row Address will change (specifically XADR7, the least significant bit).

The original RAS* signal is also sent to flip-flop U7, which is clocked by CLK to give both polarities of MUX exactly one clock cycle (78.9 nanoseconds) after RAS*.

The signal, XADR7, is an inversion of CRTCLK, therefore, the most significant X address will have two values for each CRTCLK cycle. This is of paramount importance for the page

read and write cycles of the DRAM to work, which is how we get by with only a four bit wide DRAM array. This signal is also used to toggle the Nybble Write Multiplexer (in order) to each nybble of data into its own RAM address.

The signal STROBE* occurs when QA and QB are high and CLK is low. This occurs once for each four CLK cycles, or twice for each CRTCLK. Note that it occurs just prior to the transition of XADR7. This signal is used to load the dot information into the Shift Register. It is also inverted by U12, pin 6 and used to latch the least significant nybble of data into the Nybble Read Latch.

The inverter is used to insure that the falling edge of STROBE* latches the data into the Nybble Read Latch. The uninverted (active low) version of this signal is used to load the data into the Shift Register so that the load will be finished by the next positive transition of CLK. Part of U1 is used to delay the CLK signal into the PAL so that it arrives at approximately the same time as the QA, QB, and QC inputs.

The rest of the timing (refer to Graphics Board Read/Write Timing Chart, Figure 5) is controlled by another PAL, U14 (16R4). This is referred to on the Block Diagram as the CPU Handshake Logic. U14 is a registered PAL which uses MUX* as a clock. The outputs we are concerned with for this portion are: Q*, WAIT*, VWR*, VDCPU, and RDLATCH. The Q* output is an intermediate signal point, and is not used externally to the PAL. It is, however, a term in some of the internal equations and is therefore necessary.

During a CPU read cycle, the first thing that happens is that VIDRAMRD* goes low. Immediately, this causes the WAIT* output to go low because Q* is currently high. This immediately causes the Z8Ø to go into a wait state, insuring that VIDRAMRD* will remain low. On the next falling edge of MUX, Q* goes low. If, at this time, either VSYNC or HSYNC is high, VDCPU will also go high. Remember that this signal is used to switch the multiplexers to allow CPU addresses to reach the DRAM array.

The equation for VDCPU is so set up that it will latch for only one MUX* cycle. Therefore, on the next rising edge of MUX*, VDCPU returns to a low. Simultaneously, because VDCPU was high at the instant of the MUX* transistion, RDLATCH will go high - again for one MUX* cycle. The rising edge of this signal is used to latch the current data nybble, as well as the nybble in the Nybble Read Latch, into the Byte Read Latch.

Meanwhile, the WAIT* signal has been maintained until the rising edge of RDLATCH because of the portion of the WAIT* equation: RDLATCH* AND WAIT*. As soon as the rising edge of RDLATCH occurs, this equation is no longer satisfied, and the WAIT* signal goes away, releasing the Z8Ø to complete the Read cycle.

The Read cycle is much the same if VSYNC and HSYNC are both low, except that VDCPU, and therefore RDLATCH, do not happen until the first rising edge of MUX* after one of these signals goes high. In this case, the WAIT* signal is extended until either VSYNC or HSYNC goes active. This prevents the CPU from accessing the DRAM during the active portion of the display, and thus eliminates streaking.

The Write cycle is the same as the Read cycle, except that the PAL has the input VIDRAMWR* active and, upon the rising edge of VDCPU, it forces VWR* active.

Video Output

The Q outputs from the DRAM array are fed to the four most significant inputs of U16 which is a parallel-load, serial-out Shift Register. It is capable of loading and shifting eight bits at a time, but in this application, only four are used. At the rising edge of the first CLK input after a load, the H input is transferred to the QH output. Simultaneously, all other inputs are moved towards H. (G becomes H, F becomes G, etc.) At the rising edge of the next CLK input, the new H is output to QH, and so forth.

After four CLK pulses a STROBE* occurs, loading four new bits into the parallel inputs. The QH output becomes the dot stream for video output. However, it is ANDed with a version of DISENB that has been delayed for two STROBE* cycles (one eight-position character cycle) by the Nybble Read Latch. The AND gate is U22, pin 11 (74LSØ8). DISENB is the display enable output of the CRTC, which goes low during horizontal and vertical retrace. This insures that dot information is only output during the active portion of the display.

This active dot stream is sent to a quad one-of-two multiplexer, U32 (74LS157). When the select input to this multiplexer is high, this dot stream will be transferred to one of the outputs of U32.

Other inputs which will also be transferred to their respective outputs when the select input is high are HSYNC and VSYNC* (both from the CRTC) and they are inverted by U28, pin 6. VSYNC is inverted because the video monitor in the Model III requires a negative going vertical sync.

The inputs to the other section of the multiplexer are the video and sync outputs of the Model III standard video display circuitry. The signal which is used to select which side of the multiplexer is active is called GRAPHICS/ALPHA*, and comes from the Options Register.

Options Register

The Options Register consists of an eight-bit latch, U15 (74LS273), and part of PAL U14. The Clear input of the latch is tied to buffered RESET* to insure that all options are cleared on power up or reset. An OUT to port 8Ø Hex clocks the data that is output into the latch. The following bit map lists the function of each bit:

PORT 8Ø (Hex) BIT MAP

Bit	Function
ØØ	GRAPHICS/ALPHA*
Ø1	Not used
Ø2	X Register Decrement/Increment*
Ø3	Y Register Decrement/Increment*
Ø4	Read X Register Sit/Clock*
Ø5	Write X Register Sit/Clock*
Ø6	Read Y Register Sit/Clock*
Ø7	Write Y Register Sit/Clock*

The GRAPHICS/ALPHA* signal selects which side of the video output multiplexer is active. The X,Y Decrement/Increment* lines go to the Down/Up* pins on the appropriate counter registers (U17 - U2Ø). Bits 4 through 17 connect to PAL U14.

Inside the PAL these signals are combined with VIDRAMRD* and VIDRAMWR* to generate the clock signals that increment or decrement the appropriate X,Y Counter registers. (Refer to the PAL equations at the lower left corner of Sheet two of the Schematic Diagram.) These indicate that at least one of the four most significant bits must be clear in order for any automatic incrementing or decrementing of the X,Y Counters to take place.

For example, if bit two is set and bit 4 is reset prior to a VIDRAMRD*, the XCLK output from the PAL will be high. When VIDRAMRD* occurs, XCLK will go low. As VIDRAMRD* returns to its inactive state, XCLK will return high, thus decrementing the X Counter registers. (Note that if bit two had been reset, the X Counter would have been incrementing instead of decrementing.) If bits four through seven are all set, the XCLK and YCLK outputs of the PAL will remain high, regardless of the state of VIDRAMRD* and VIDRAMWR*.

4/ Installation

Note:
The Model III that you are working on must have 48K of RAM and one disk drive.

Case

1. Remove all cables from the bottom and rear of the Computer. Position the Computer on its rear panel to provide easy access to the Case Bottom. Remove the ten screws from the Case Bottom. Notice the different types and lengths of screws and note their positions. Set them aside in groups.

2. Position the Computer upright and remove the #6 screw and washer from the top, Back Panel of the Case.

3. Very carefully remove the Case Top by lifting it straight up, then set it aside to your left (when facing the CRT). Be careful not to exceed the length of the video cable.

CPU Board

1. Remove all cables connecting the CPU Board: the power supply cable, video, keyboard, and cassette cables. If applicable, also remove the RS-232 and FDC inter-connect cables. (Refer to Figure 1.)

2. Remove the five screws that secure the PC Board.

3. Remove the small PCB Mounting Bracket and its two screws from the top of the metal chassis bracket.

4. Make sure that all cables to the CPU Board have been disconnected.

5. Remove the CPU Board.

5/ P.C. Board Interconnections

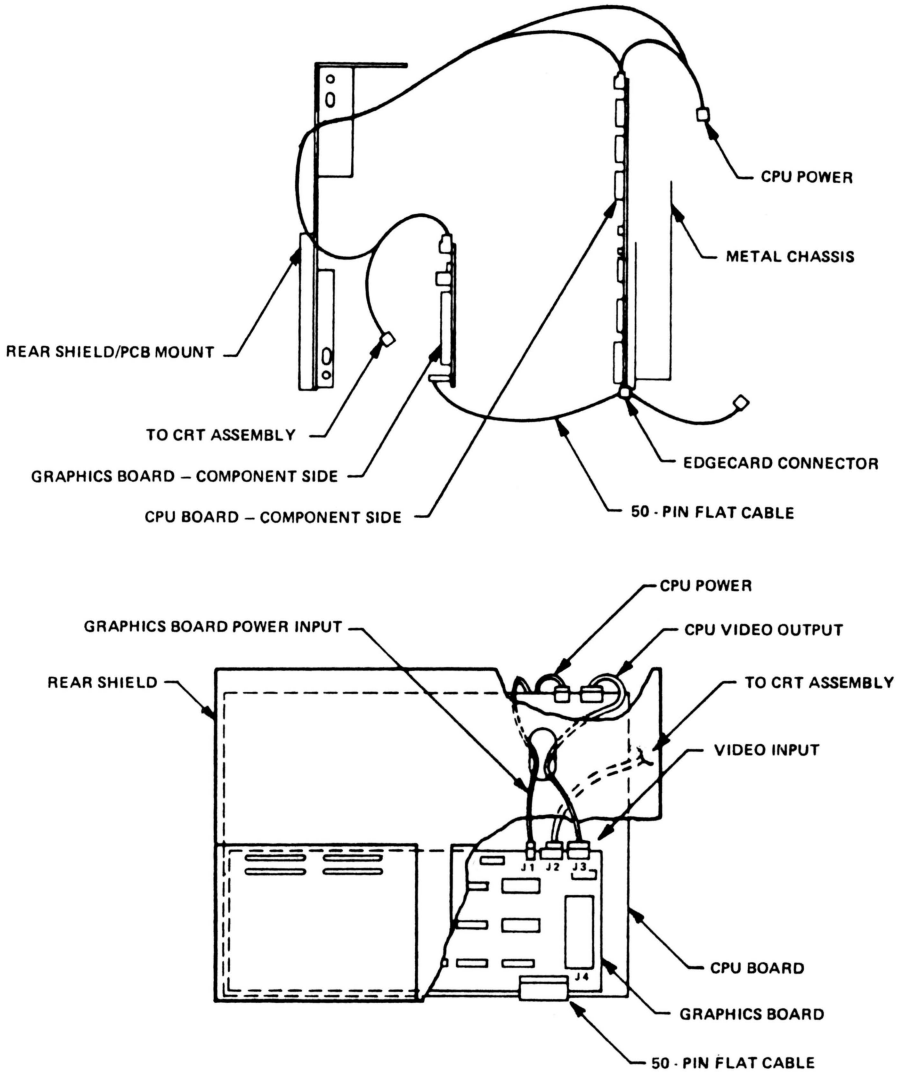


Figure 1 PC Board Interconnections

CPU Modification:

1. Cut pin 1 of U1Ø3 away from the Board. This is **not** a trace cut. (Refer to Figure 2 for details.)

2. Connect the cut-away pin (**not** the PCB trace) to ground (a ground point that is close to U1Ø3 is pin 7 of U87).

Graphics Board Installation

1. Connect the 5Ø-pin flat cable to the CPU Board at J2 (the I/O Bus Connector) and to the Graphics Board at J4. The middle edge-card connector plugs into J2. (Refer to Figure 1.)

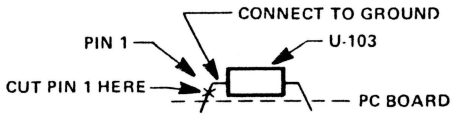
Notes:
The edge-card connector must be firmly seated in its socket. Connecting and disconnecting peripheral devices could easily loosen the edge-card connector which would give a false indication of a malfunction.

When connecting and disconnecting peripheral devices, make sure that the male to male connector remains with the plug on the 5Ø-pin flat cable.

2. Replace the CPU Board in the Case. The third connector of the 5Ø-pin flat cable exits the Case through the opening for the I/O bus.

3. Replace the mounting screws that were removed from the CPU Board.

4. Make sure that all components on the Graphics Board assembly are in place. The Graphics Board should be attached to a new back shield for the CPU Board, and there should be three layers of material attached to the back of the Graphics Board. Two layers are the insulator and ground plane for the Graphics Board. The third layer is the insulator (clear tape) that prevents the CPU from shorting against the Graphics Board ground plane.



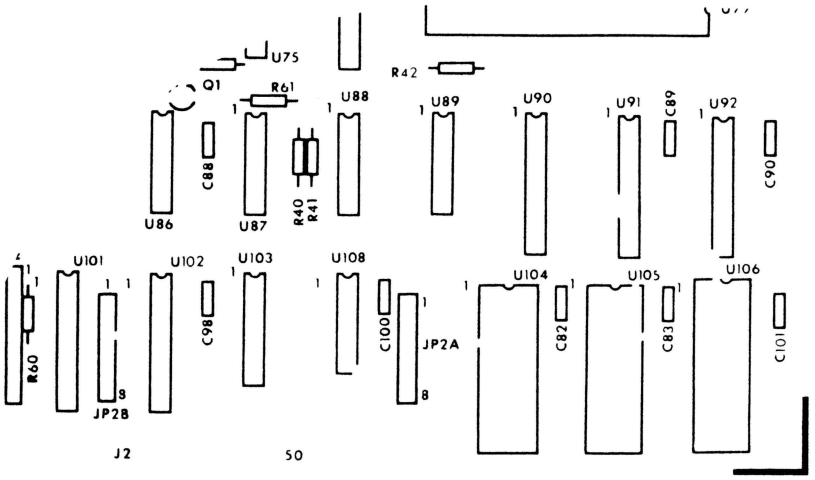


Figure 2. CPU Board Modification

5. Connect the remaining cables to the Graphics Board and the CPU. The short six-pin jumper cable connects the video output of the CPU (J5) to the Graphics Board video input (J3). The video cable from the CRT assembly connects to the Graphics Board video output (J2).

6. The final cable supplied with the Graphics Board is a replacement for the power cable from the Power Supply to the FDC interface board, and has an additional connector for the Graphics Board. Remove the old power cable to the FDC and replace it with the new cable. The extra two-pin connector plugs into the Graphics Board power input (J1).

7. Place the Graphics Board and shield assembly in the proper position and reconnect the shield with the screws that were removed from the old shield. Note: If this modification is being made to an older, non-FCC approved (no rear shield) Model III, use the holes that do line up on top of the shield. Spring clamps will be used to secure the edges.

8. It is possible that, after installation of the Graphics Board, the video display would be too large for the CRT. If this happens, adjust the horizontal and vertical size and the horizontal and vertical linearity. (Refer to the Model III Technical Reference Handbook, Section VII Video Monitor CRT, Figure 3 and Part H under **Service Adjustments.**)

Case

1. Double-check to be sure that all wires are connected correctly and all Boards are properly fastened.

2. Carefully place the Case Top over the Case Bottom. **Do not hit the CRT neck. It could implode or break off.**

3. Install the #6 x 3/8" sheet metal screw and flat washer in the top rear panel of the Case.

4. Carefully rest the Computer on its rear panel and replace the ten #8 screws/ five 1" sheet metal toward the rear, three 7/8" machine head along the front, and two 1" machine head in the remaining positons.

Checkout

1. Power up the system and verify proper operation with the available diagnostics.

6/ Block Diagram

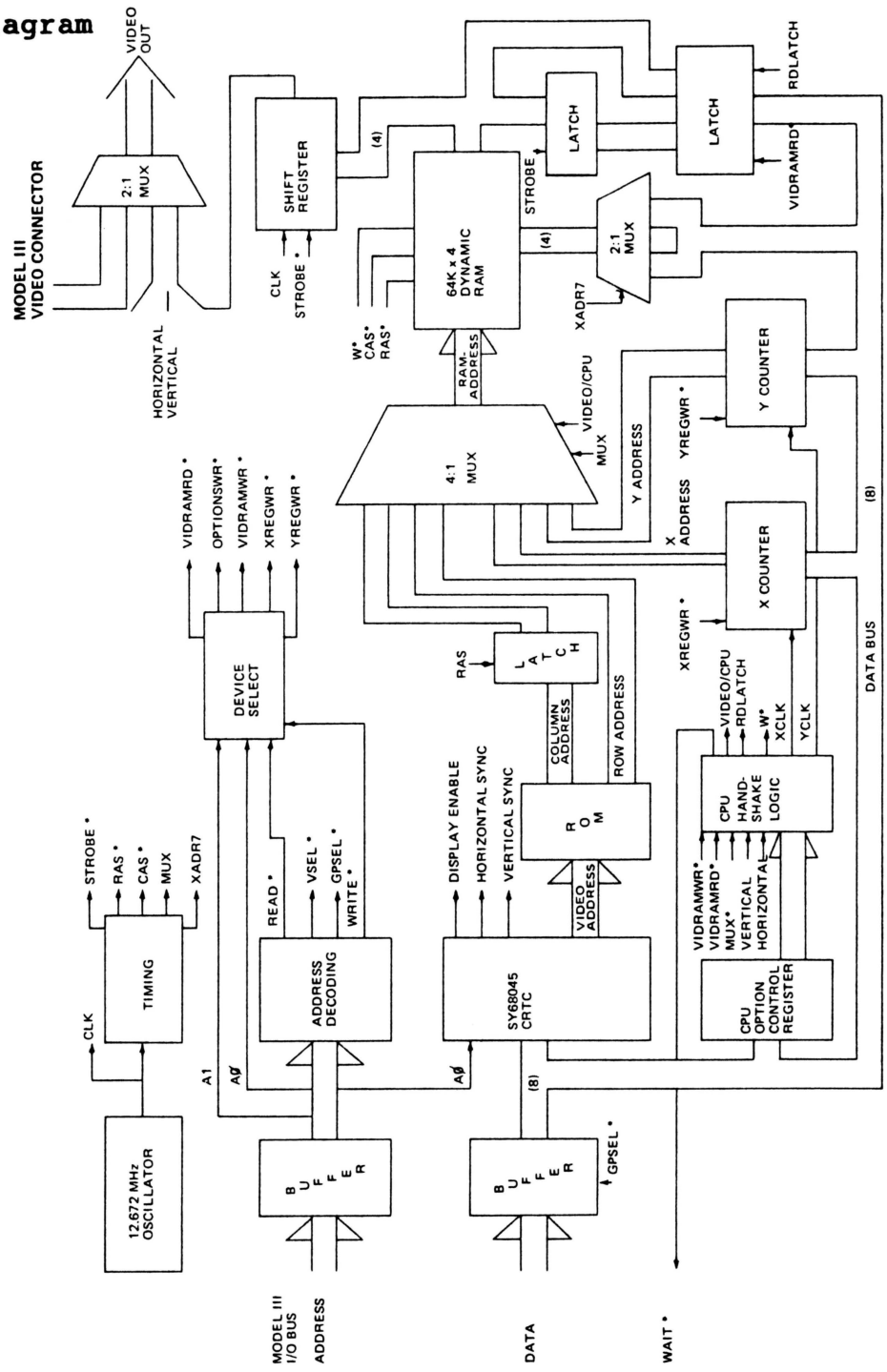


Figure 3. Model III Graphics Block Diagram

7/ Troubleshooting

New Installation

If the Model III or the Graphics Board is inoperative following a new installation, chances are that the problem is associated with the installation procedure. Recheck all connections. Insure that the ribbon cable is properly seated on both the Model III CPU Board and the Graphics Board. Verify that power is connected to the Graphics Board. Make sure that the video cable from the Model III is plugged into the connector closest to the edge of the Graphics Board (J3) and that the cable to the CRT harness is on the center connector (J2).

Double check the Modification to the Model III CPU. Finally, make sure that the Graphics Board is not shorted to either the Model III CPU Board or the shield. Inspect all cables for broken insulation or punctures. Re-seat all of the socketed IC's on the Graphics Board. If you are satisfied that all of this is correct, have someone else check your work. If you still have problems, try another Graphics Board to insure that the problem is not in the Model III. Once you have determined that the problem is definitely in the Graphics Board, re-install it and go to the next section.

In Service Failure

On a working unit that has failed, you can assume that the installation is correct and that a component on the Graphics Board has failed. The following pages contain flowcharts for troubleshooting almost any defect on the Graphics Board down to the component level. These flowcharts assume that you have an oscilloscope of at least 15 MHz bandwidth. The flowcharts also assume that the defect is caused by a faulty component, as it is almost impossible to anticipate every combination of shorted or open traces on the circuit board.

So it is up to you to check visually, and with an ohmmeter if necessary for this type of failure. The Troubleshooting charts can be used to a limited degree even in these cases. For example, if the chart leads you to a component, and replacement of the component does not eliminate the problem, then it is likely that there is a PCB short or open associated with one or more of the pins on that component.

When troubleshooting by use of flowcharts, you should not, for example, attempt to troubleshoot the sit-run registers until the video RAM write and read checks have been performed. Two symptoms that are not covered by the flowcharts due to the extreme shortness of the chart are:

Missing or extra pixels —— Replace the RAM chips.

CPU "hangs up" when attempting to write or read Graphics RAM —— Replace the PAL U14.

To use some of the flowcharts, you must load and execute the appropriate programs to exercise certain portions of the Graphics Board circuitry. However, in the absence of the diagnostic package, the programs can be written by you if you are familiar with Z8Ø Assembly language and the Theory of Operation of the Graphics Board. (You cannot use BASIC to generate signals on an oscilloscope because of its slow speed and low repetition rate.) Below is a sample program to exercise the Options Register:

```
            ORG    6ØØØH          ; Put it out of the way of OS
;
    START   LD     A,Ø55H         ; Set every other (odd) bit
            OUT    A,Ø8ØH         ; Write it to the Options
                                    Register
            LD     A,ØAAH         ; Set every other (even) bit
            OUT    A,Ø8ØH         ; Write to O. R.
            JR START              ; Loop until reset
;
            END
```

One Final Note: If the Graphics Board you are working on contains a 6845 CRTC chip, as opposed to 68Ø45, then the chip **must be initialized** by the appropriate software before checking out the Graphics Board.

See the "Troubleshooting Charts" in Appendix A for additional information.

8/ Timing Chart

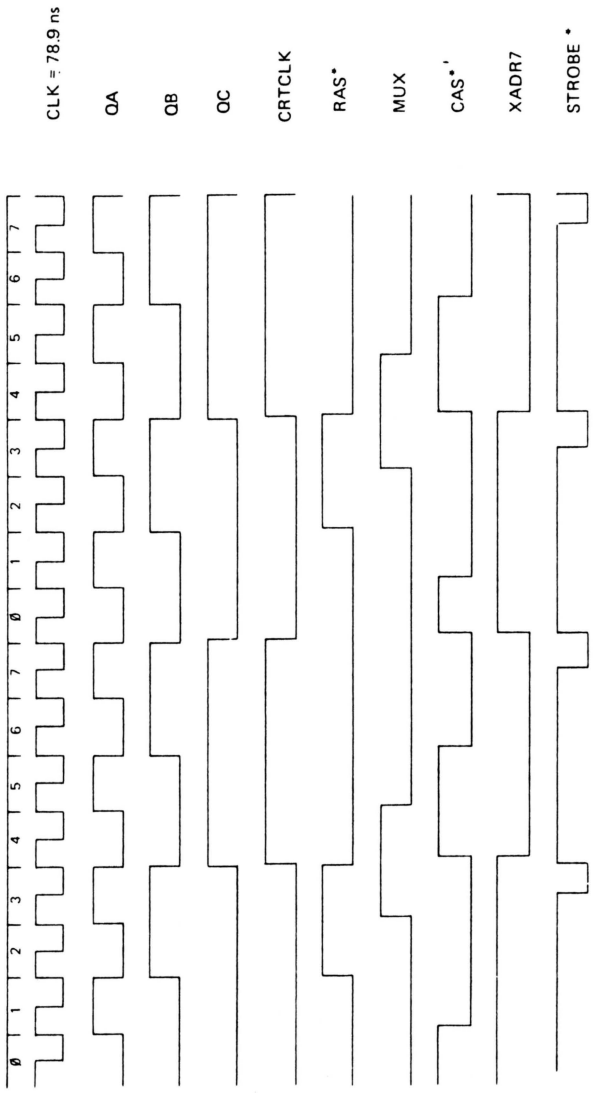


Figure 4. Memory Timing Chart

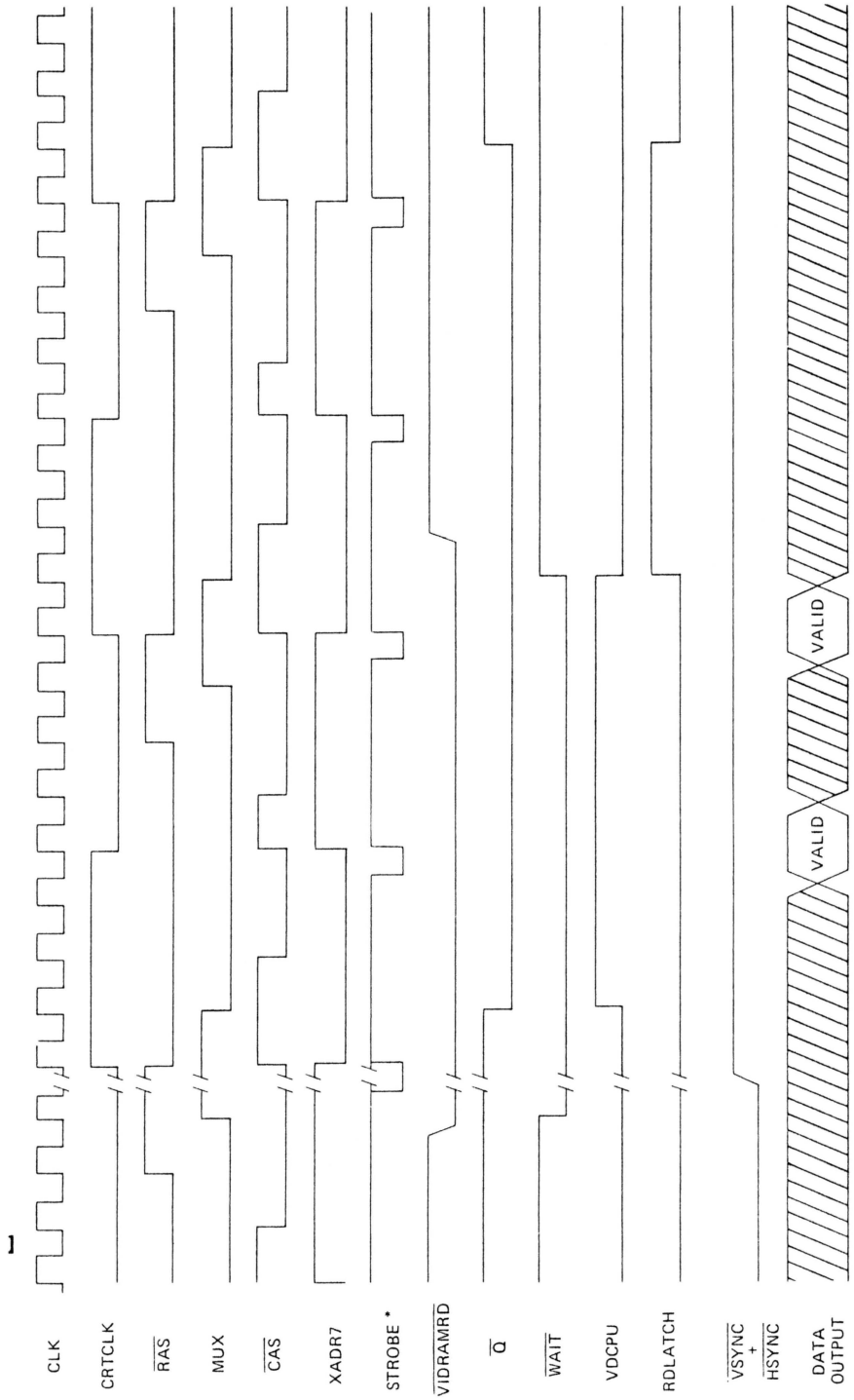


Figure 5. Graphics Board Read/Write Timing

9/PCB Art

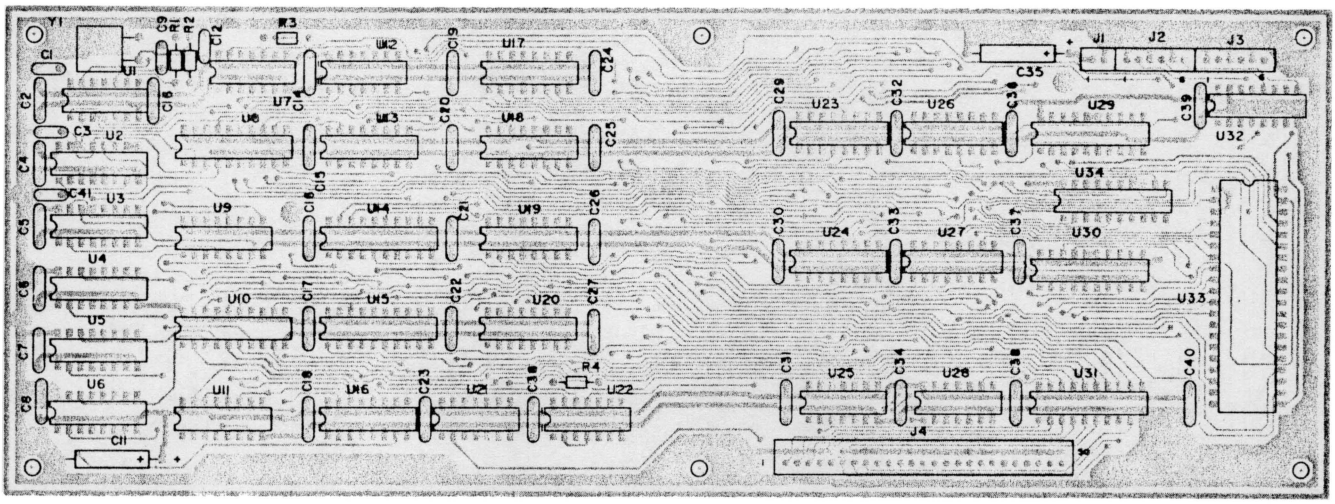


Figure 6. P.C. Board (Top "X-ray" View)

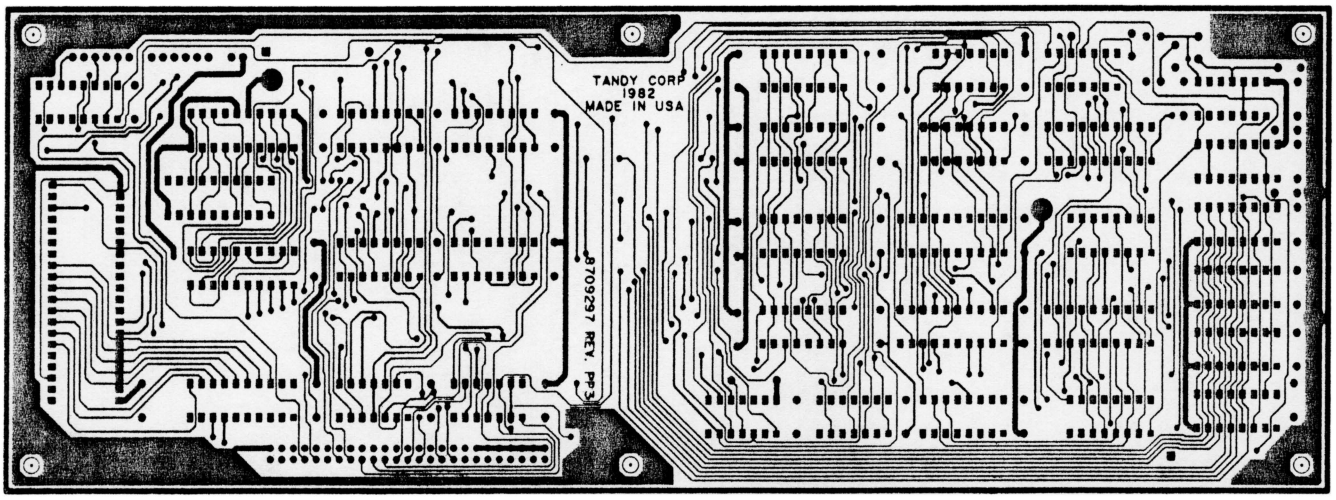
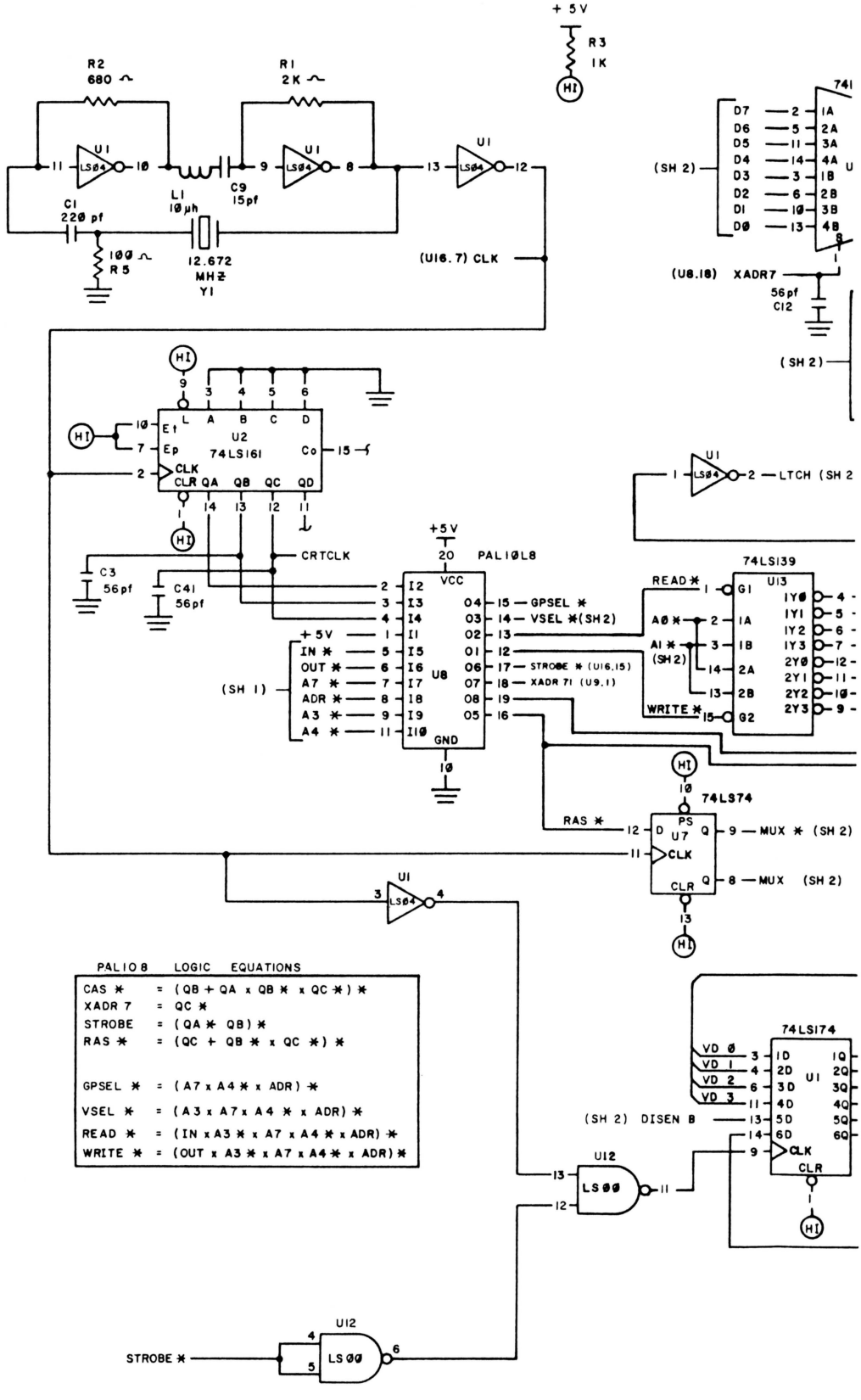


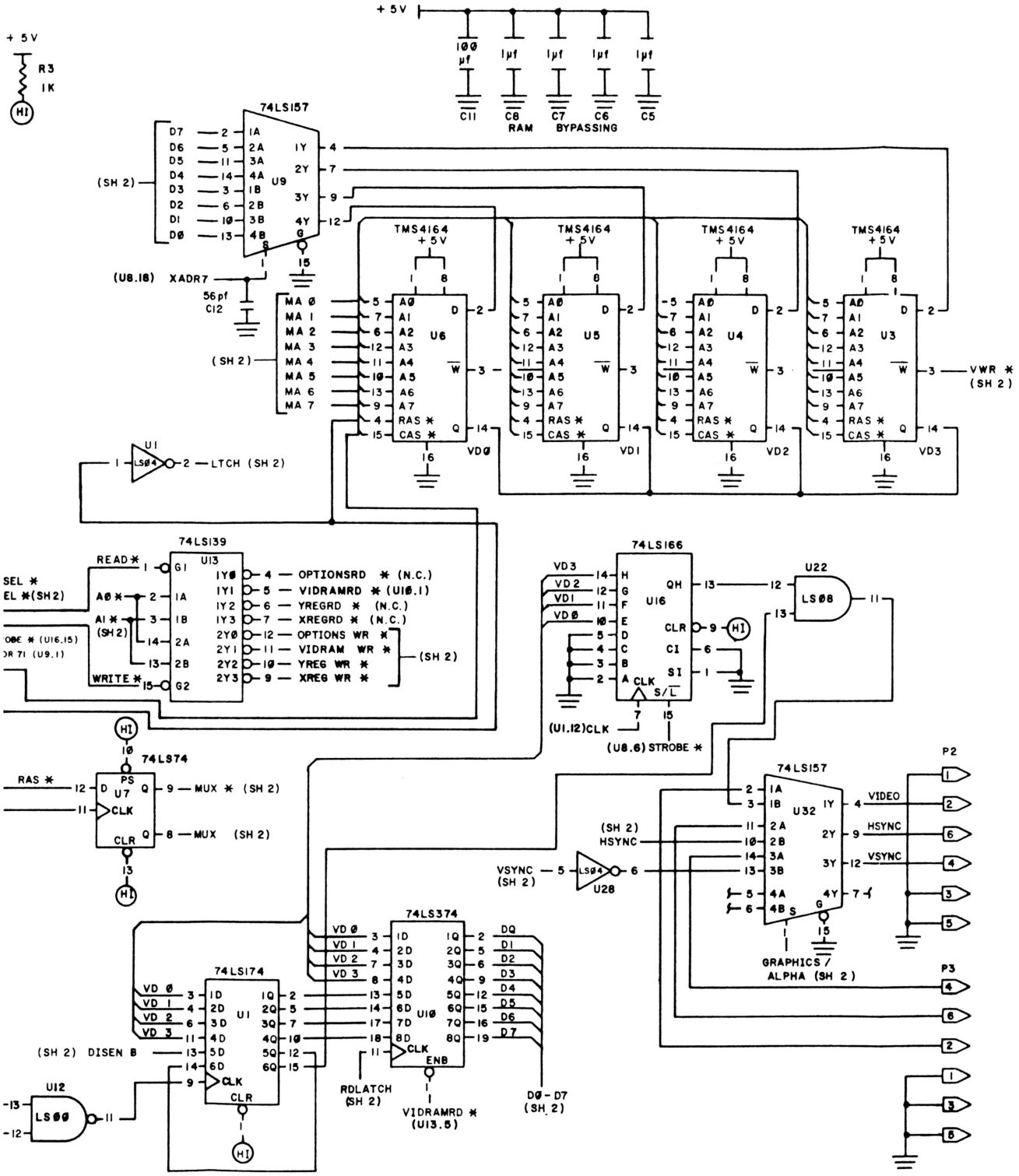
Figure 7. P.C. Board (Bottom View)

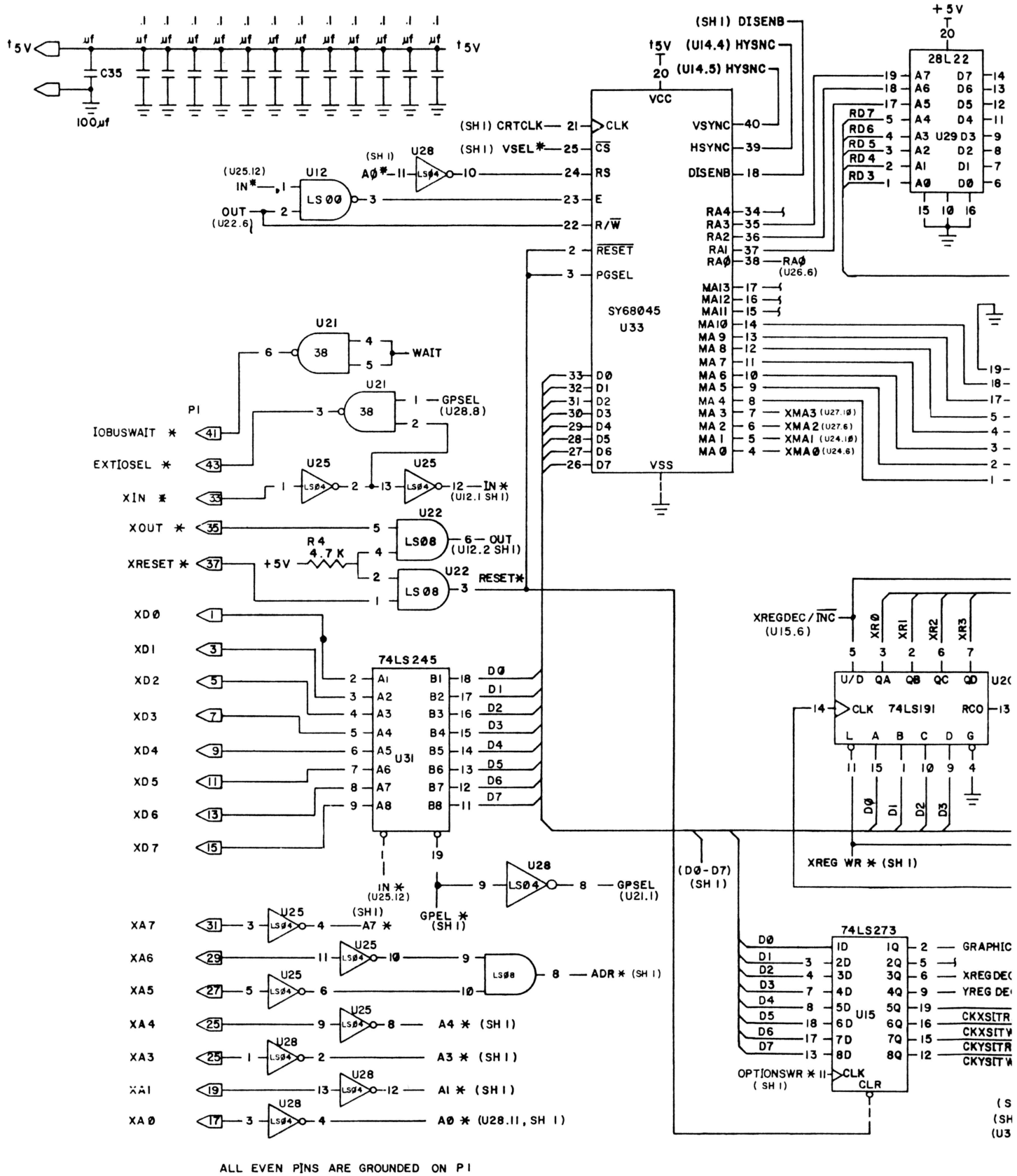
1Ø/ Parts List

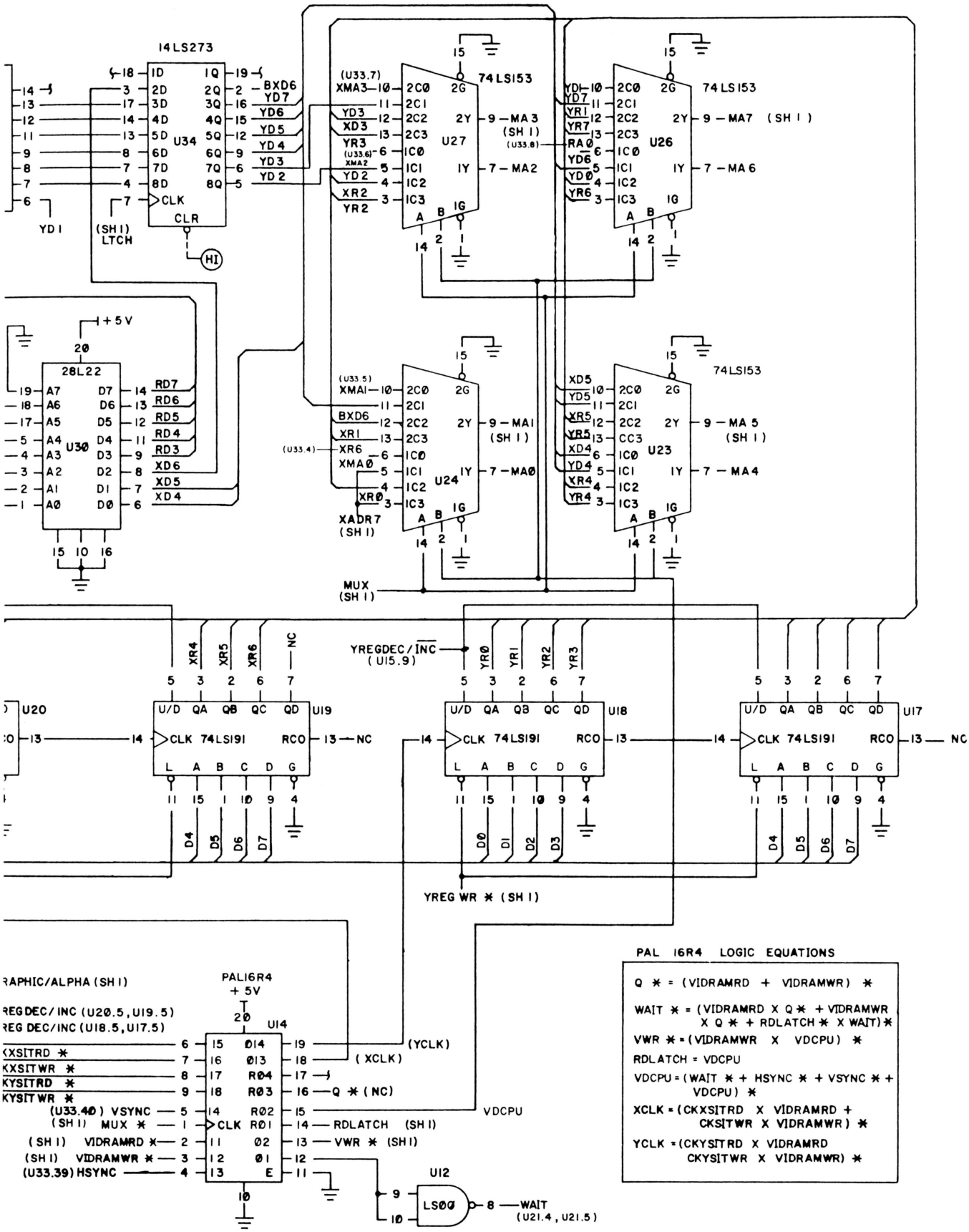
Symbol	Description	PartNumber
Capacitors		
C1	15pF, 5ØV, Ceramic Disk	83ØØ153
C2,4-8,1Ø	Ø.1µF, 5ØV, Mono Axial	8374ØØ4
C14-34,36-4Ø		
C3,12,41	56pF, 5ØV, Ceramic Disk	83ØØ564
C9	Ø.ØØ1µF, 5ØV, Mono	8383ØØ4
C11,35	1ØØµF, 16V, Electrolytic, Axial	8317ØØ1
Connectors		
J1	Power, 2-pin, Right Angle	8519113
J2,3	6-pin, Right Angle	8519ØØ3
J4	Header, Male, 25 Dual Double Row	8519117
Crystal		
Y1	12.672MHz	84Ø9Ø25
Integrated Circuits		
U1,25,28	74LSØ4, Hex Inverter, 14-pin	8Ø2ØØØ4
U2	74LS161, Binary Counter, 16-pin	8Ø2Ø161
U3-U6	TMS4164, RAM, 64K, 15Øns, 16-pin	8Ø41665
U7	74LS74, Dual Flip-Flop, 14-pin	8Ø2ØØ74
U8	PAL1ØL8, 2Ø-pin	8Ø754Ø8
U9,32	74LS157, Quad Data Selector, 16-pin	8Ø2Ø157
U1Ø	74LS374, Octal Flip-Flop, 2Ø-pin	8Ø2Ø374
U11	74LS174, Hex Flip-Flop, 16-pin	8Ø2Ø174
U12	74LSØØ, Quad 2-input NAND, 14-pin	8Ø2ØØØØ
U13	74LS139, Decoder, 16-pin	8Ø2Ø139
U14	PAL16R4, 2Ø-pin	8Ø75164
U15,34	74LS273, Octal Flip-Flop, 2Ø-pin	8Ø2Ø273
U16	74LS166, Shift Register, 16-pin	8Ø2Ø166
U17-2Ø	74LS191, Binary Counter, 16-pin	8Ø2Ø191

Symbol	Description	Part Number
U21	7438, Quad 2-input NAND, 14-pin	8ØØØØ38
U22	74LSØ8, Quad 2-input AND, 14-pin	8Ø2ØØØ8
U23,24,26,27	74LS153, Data Selector, 16-pin	8Ø2Ø153
U29	28L22, Bipolar Y ROM, 2Ø-pin	8Ø75122
U3Ø	28L22, BIPOLAR X ROM, 2Ø-pin	8Ø75Ø22
U31	74LS245, Octal Transceiver, 2Ø-pin	8Ø2Ø245
U33	SY68Ø45,4Ø-pin	8Ø4ØØ45
Resistors		
R1,2	47Ø ohm, 1/4W, 5%	82Ø7147
R3	1K, 1/4W, 5%	82Ø721Ø
R4	4.7K, 1/4W, 5%	82Ø7247
Sockets		
U3-6	16-pin	85Ø9ØØ3
U8,14,29,3Ø	2Ø-pin	85Ø9ØØ9
U33	4Ø-pin	85Ø9ØØ2
Miscellaneous		
	RFI Shield, Back Cover, Sheet Metal	8729136
	RFI Shield, Graphics Mylar	8539Ø22
(8)	Fasteners, Tri-Mount	8559Ø23
	P.C. Board	87Ø9297
	Flat Ribbon Cable, 5Ø-pin (I/O Bus)	87Ø9338
	Video Cable, 6-pin, Polarized	87Ø9337
	FDC/Graphics Power Cable, 2-pin	87Ø9363
	P.C. Board Adapter	87Ø9323
	Diskette, Graphics	8792Ø49
	Label, Upgrade	8789734
	Manual, Service	8749431
(5)	Screw, #6 x 1/4, Sheet Metal	8
	Screw, #6 x 1/4, Machine	8569Ø98
(6)	Screw, #6 x 3/8, Sheet Metal	8569128
(4)	Spring Clip	8559Ø52


+ 5V
R3
1K
R2
680
R1
2K
U1
LS04
L1
10µh
C9
15pf
C1
220 pf
100
R5
12.672
MHZ
Y1
(U16.7) CLK
(SH 2)
(U8.18) XADR7
56pf
C12
U2
74LS161
CLK
CLR
QA
QB
QC
QD
CRTCLK
C3
56pf
C41
56pf
PAL10L8
U8
GPSEL *
VSEL *(SH2)
STROBE * (U16,15)
XADR 7! (U9,1)
(SH 1)
IN *
OUT *
A7 *
ADR *
A3 *
A4 *
74LS139
U13
READ *
A0 *
A1 *
WRITE *
LTCH (SH 2
74LS74
U7
RAS *
MUX * (SH 2)
MUX (SH 2)
PAL10 8 LOGIC EQUATIONS
CAS * = (QB + QA x QB * x QC *) *
XADR 7 = QC *
STROBE = (QA * QB) *
RAS * = (QC + QB * x QC *) *
GPSEL * = (A7 x A4 * x ADR) *
VSEL * = (A3 x A7 x A4 * x ADR) *
READ * = (IN x A3 * x A7 x A4 * x ADR) *
WRITE * = (OUT x A3 * x A7 x A4 * x ADR) *
74LS174
VD 0
VD 1
VD 2
VD 3
(SH 2) DISEN B
U12
LS00
STROBE *

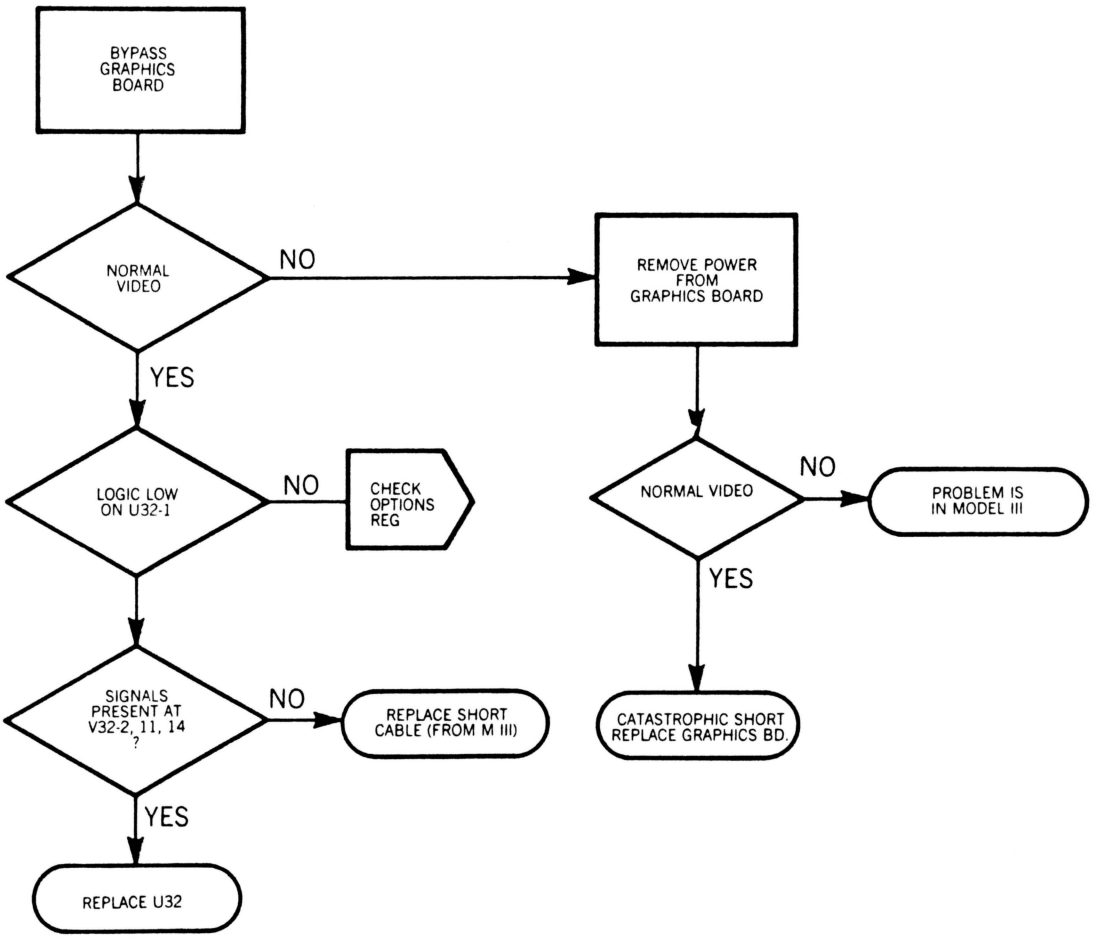

+ 5V
R3
1K
HI
+ 5V
100 µf
1µf
1µf
1µf
1µf
C11
C8
C7
C6
C5
RAM
BYPASSING
74LS157
U9
(SH 2)
D7
D6
D5
D4
D3
D2
D1
D0
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
S
G
(U8.18) XADR7
56pf
C12
TMS4164
+ 5V
U6
U5
U4
U3
MA Ø
MA 1
MA 2
MA 3
MA 4
MA 5
MA 6
MA 7
(SH 2)
AØ
A1
A2
A3
A4
A5
A6
A7
RAS *
CAS *
D
Q
W
VDØ
VD1
VD2
VD3
VWR *
(SH 2)
U1
LSØ4
LTCH (SH 2)
74LS139
U13
READ *
SEL *
EL *(SH2)
AØ *
A1 *
(SH2)
WRITE *
G1
G2
1A
1B
2A
2B
1YØ
1Y1
1Y2
1Y3
2YØ
2Y1
2Y2
2Y3
OPTIONSRD * (N.C.)
VIDRAMRD * (U1Ø.1)
YREGRD * (N.C.)
XREGRD * (N.C.)
OPTIONS WR *
VIDRAM WR *
YREG WR *
XREG WR *
(SH 2)
74LS166
U16
VD3
VD2
VD1
VDØ
H
G
F
E
D
C
B
A
QH
CLR
CI
SI
CLK
S/L
(U1.12)CLK
(U8.6) STROBE *
U22
LSØ8
74LS374
U7
RAS *
PS
D
CLK
CLR
Q
MUX * (SH 2)
MUX (SH 2)
74LS157
U32
(SH 2)
HSYNC
VSYNC
(SH 2)
U28
VIDEO
HSYNC
VSYNC
GRAPHICS /
ALPHA (SH 2)
P2
P3
74LS374
U10
VD Ø
VD 1
VD 2
VD 3
ID
2D
3D
4D
5D
6D
7D
8D
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
DQ
D1
D2
D3
D4
D5
D6
D7
CLK
ENB
RDLATCH
(SH 2)
VIDRAMRD *
(U13.5)
DØ - D7
(SH 2)
74LS174
U1
(SH 2) DISEN B
U12
LSØØ


+5V
.1µf
C35
100µf
SY68045
U33
CLK
CS
RS
E
R/W
RESET
PGSEL
VCC
VSS
VSYNC
HSYNC
DISENB
(SH 1) CRTCLK
(SH 1) VSEL*
(SH 1) DISENB
(U14.4) HYSNC
(U14.5) HYSNC
RA4
RA3
RA2
RA1
RA0
MA13
MA12
MA11
MA10
MA 9
MA 8
MA 7
MA 6
MA 5
MA 4
MA 3
MA 2
MA 1
MA 0
D0
D1
D2
D3
D4
D5
D6
D7
28L22
U29
RD7
RD6
RD5
RD4
RD3
U12
LS 00
U28
LS04
U21
38
WAIT
GPSEL (U28.8)
IOBUSWAIT *
EXTIOSEL *
XIN *
XOUT *
XRESET *
U25
U22
LS08
R4
4.7 K
OUT (U12.2 SH1)
IN * (U12.1 SH1)
RESET*
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
74LS245
U31
IN * (U25.12)
GPEL * (SH1)
GPSEL (U21.1)
(D0-D7) (SH 1)
XA7
XA6
XA5
XA4
XA3
XA1
XA0
A7 * (SH1)
ADR * (SH 1)
A4 * (SH 1)
A3 * (SH 1)
A1 * (SH 1)
A0 * (U28.11, SH 1)
XREGDEC/INC (U15.6)
XR0
XR1
XR2
XR3
U/D
QA
QB
QC
QD
CLK
74LS191
RCO
L
A
B
C
D
G
XREG WR * (SH 1)
74LS273
U15
OPTIONSWR * (SH 1)
GRAPHIC
XREGDEC
YREG DE
CKXSITR
CKXSITW
CKYSITR
CKYSITW
ALL EVEN PINS ARE GROUNDED ON P1

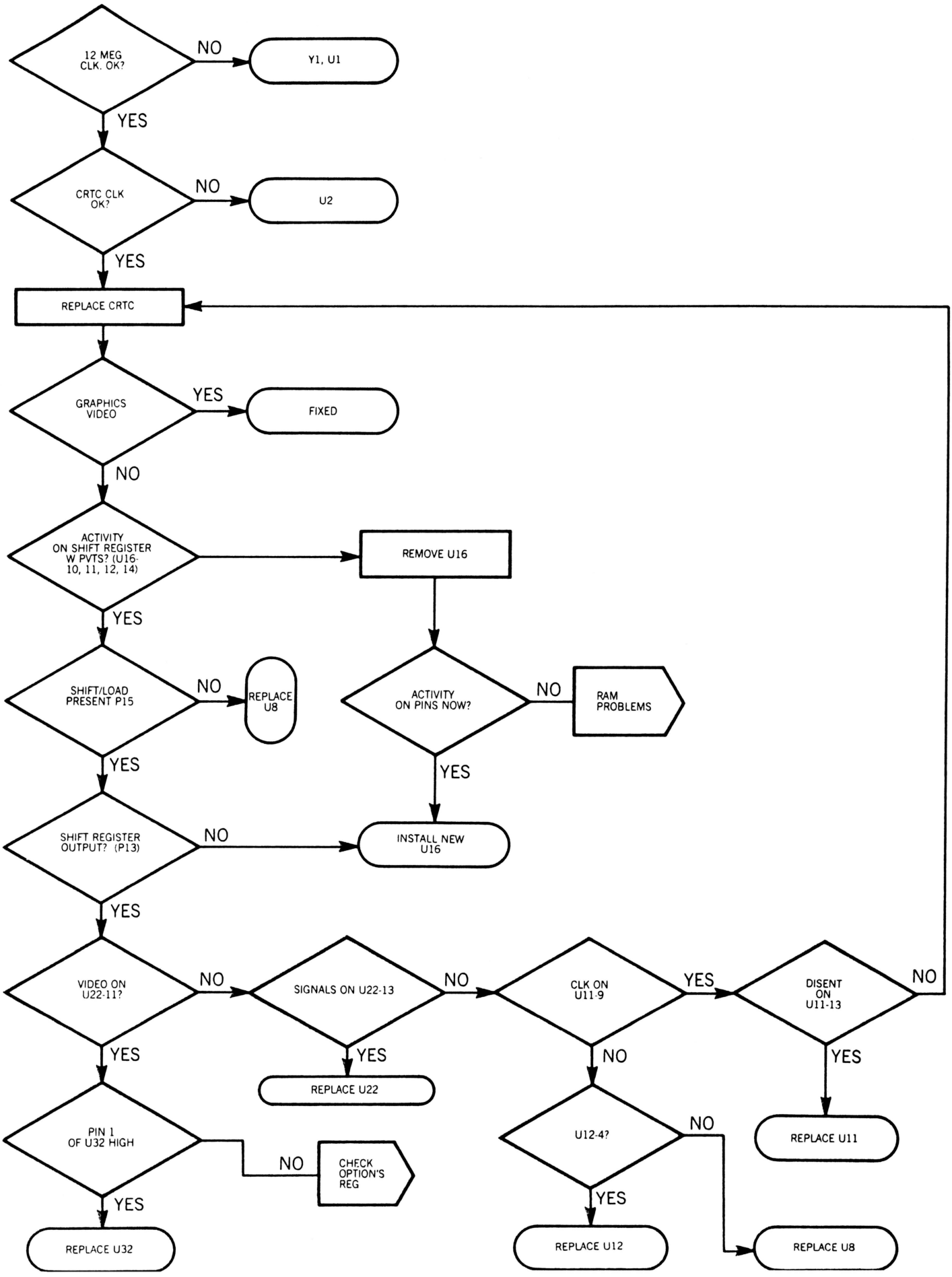

14LS273
U34
BXD6
YD7
YD6
YD5
YD4
YD3
YD2
YD1
(SH1) LTCH
CLR
HI
74LS153
U27
(U33.7) XMA3
XD3
YR3
(U33.6) XMA2
YD2
XR2
YR2
9 — MA3 (SH1)
7 — MA2
U26
YD7
YR1
YR7
(U33.8) RA0
YD6
YD0
YR6
9 — MA7 (SH1)
7 — MA6
+5V
28L22
U30
RD7
RD6
RD5
RD4
RD3
XD6
XD5
XD4
U24
(U33.5) XMA1
BXD6
XR1
(U33.4) XR6
XMA0
XR0
XADR7 (SH1)
9 — MA1 (SH1)
7 — MA0
U23
XD5
YD5
XR5
YR5
XD4
YD4
XR4
YR4
9 — MA5 (SH1)
7 — MA4
MUX (SH1)
YREGDEC/INC (U15.9)
XR4
XR5
XR6
NC
YR0
YR1
YR2
YR3
U19
U18
U17
U/D QA QB QC QD
CLK 74LS191
RCO
L A B C D G
U20
D4
D5
D6
D7
D0
D1
D2
D3
YREG WR * (SH1)
PAL 16R4 LOGIC EQUATIONS
Q * = (VIDRAMRD + VIDRAMWR) *
WAIT * = (VIDRAMRD X Q * + VIDRAMWR X Q * + RDLATCH * X WAIT) *
VWR * = (VIDRAMWR X VDCPU) *
RDLATCH = VDCPU
VDCPU = (WAIT * + HSYNC * + VSYNC * + VDCPU) *
XCLK = (CKXSITRD X VIDRAMRD + CKSITWR X VIDRAMWR) *
YCLK = (CKYSITRD X VIDRAMRD CKYSITWR X VIDRAMWR) *
RAPHIC/ALPHA (SH1)
REGDEC/INC (U20.5, U19.5)
REG DEC/INC (U18.5, U17.5)
KXSITRD *
KXSITWR *
KYSITRD *
KYSITWR *
(U33.40) VSYNC
(SH1) MUX *
(SH1) VIDRAMRD *
(SH1) VIDRAMWR *
(U33.39) HSYNC
PAL16R4
+5V
U14
(YCLK)
(XCLK)
Q * (NC)
VDCPU
RDLATCH (SH1)
VWR * (SH1)
U12
LS00
WAIT (U21.4, U21.5)

Appendix A/ Troubleshooting Charts

No Model III Video

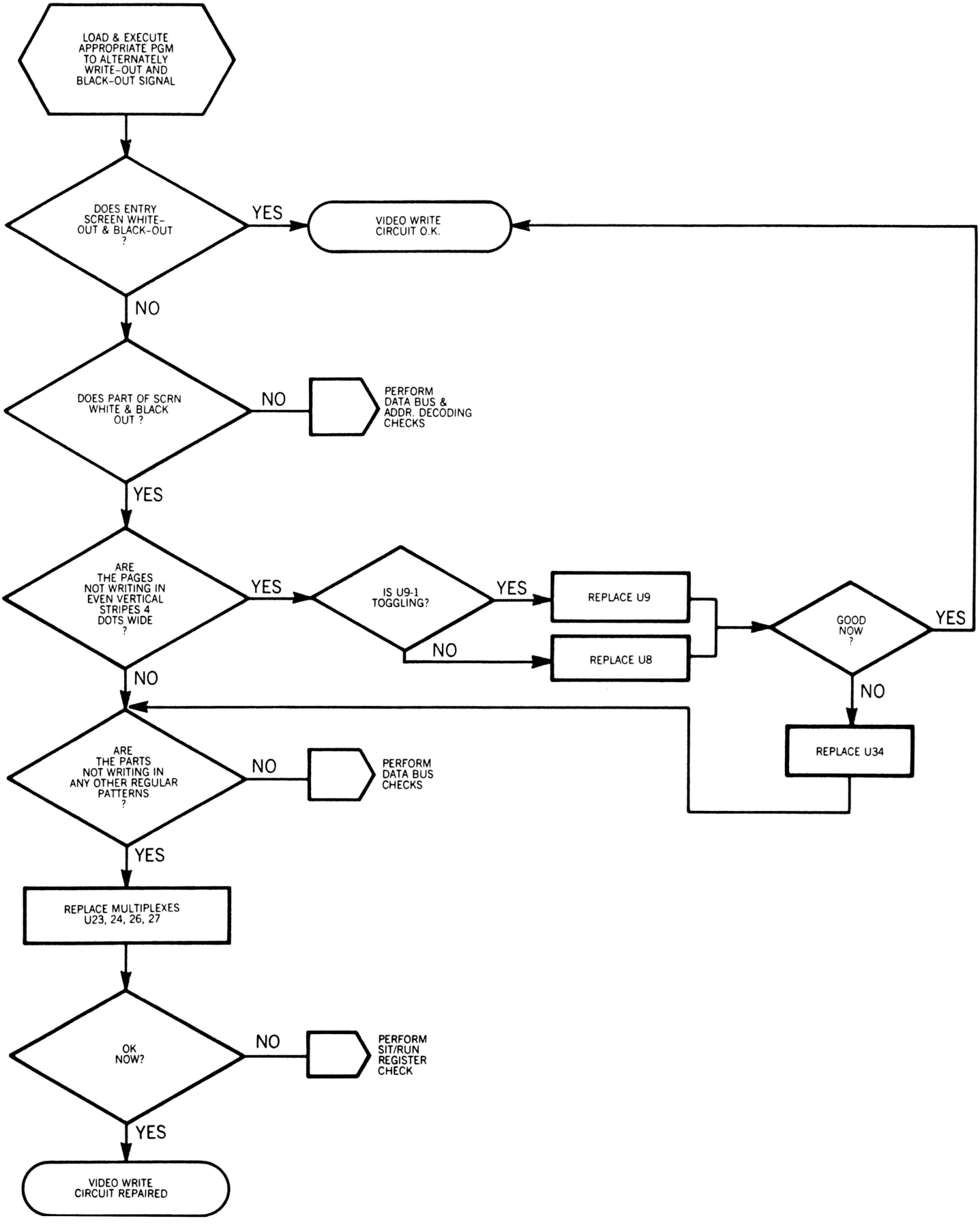


Model III Video OK, No Graphics Video



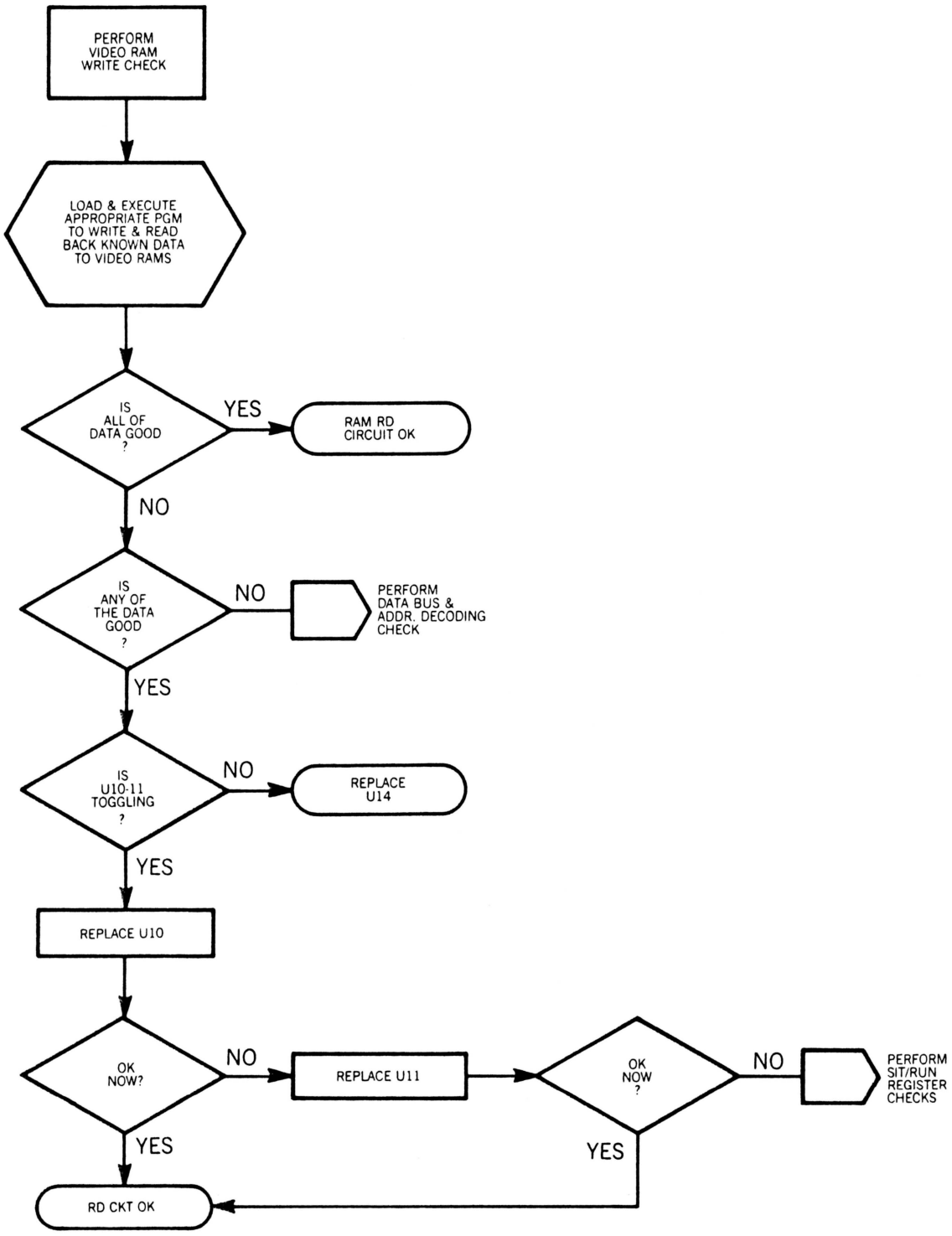
Inabililty to Write to Video ROM

Note: For any RAM-related problems always replace the RAM chips (U3-U6) with known good RAMs **before** proceeding.

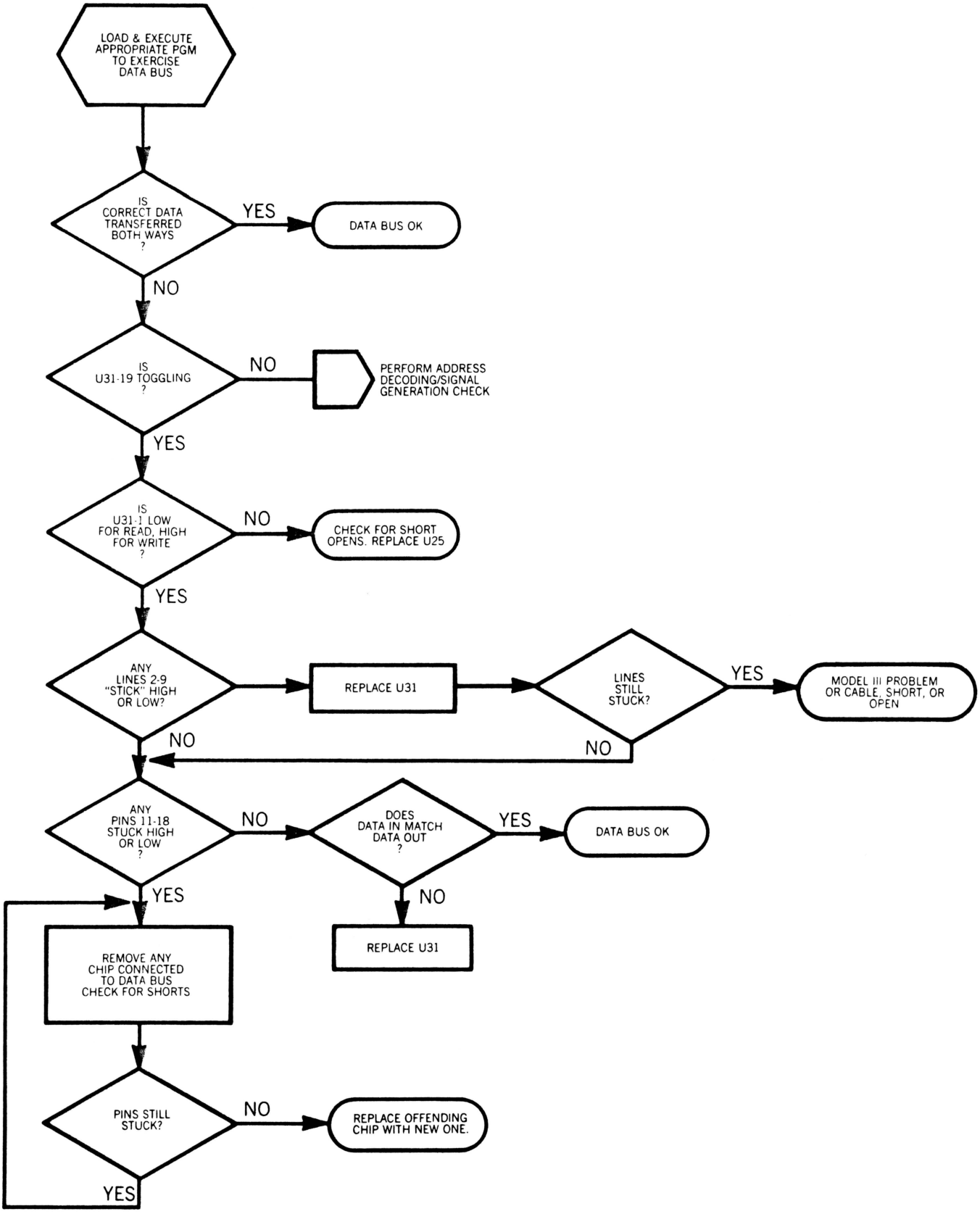


Inabiltiy to Read From Video RAM

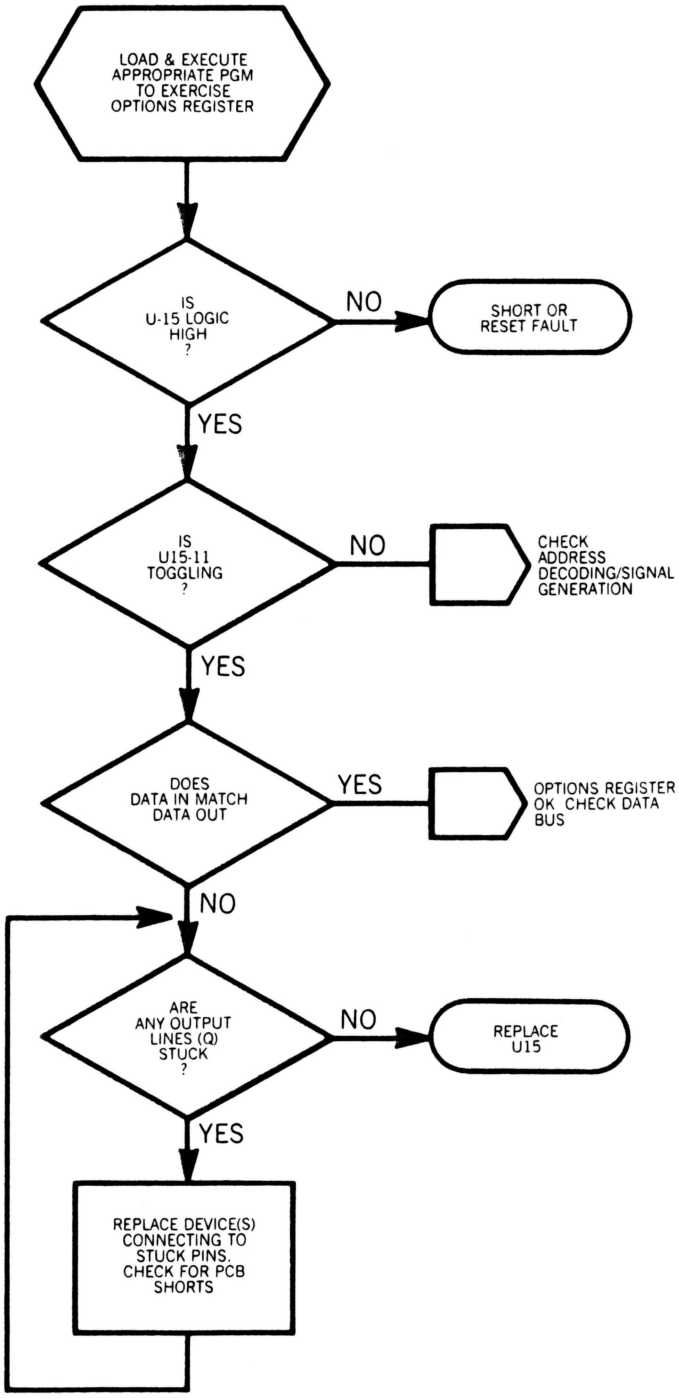
Note: For any RAM-related problems always replace the RAM chips (U3-U6) with known good RAMs **before** proceeding.



Data Bus Check

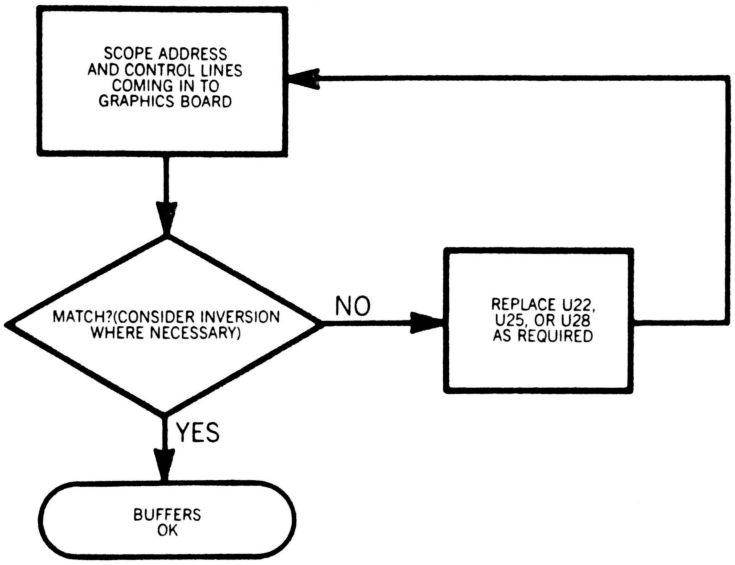


Options Register Check

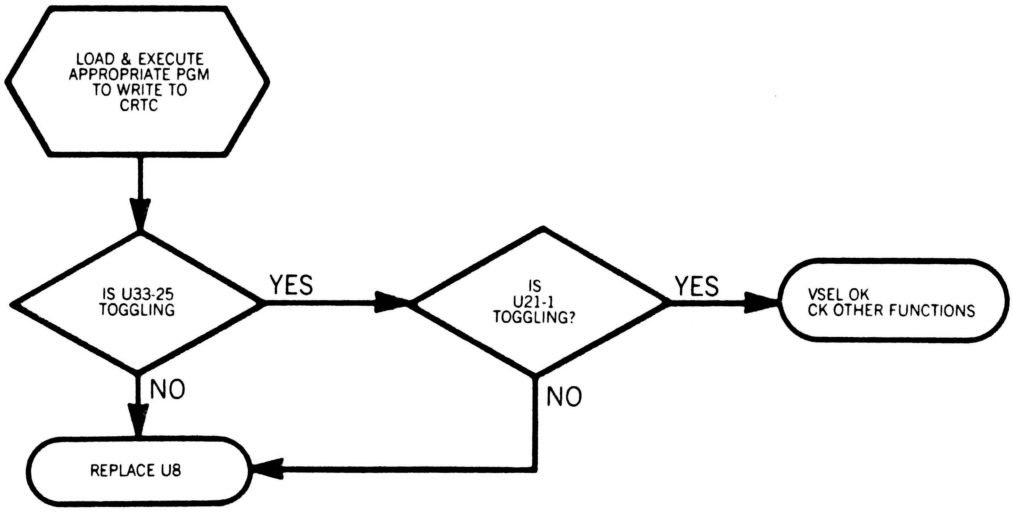


Address Decoding/Device Selection Check

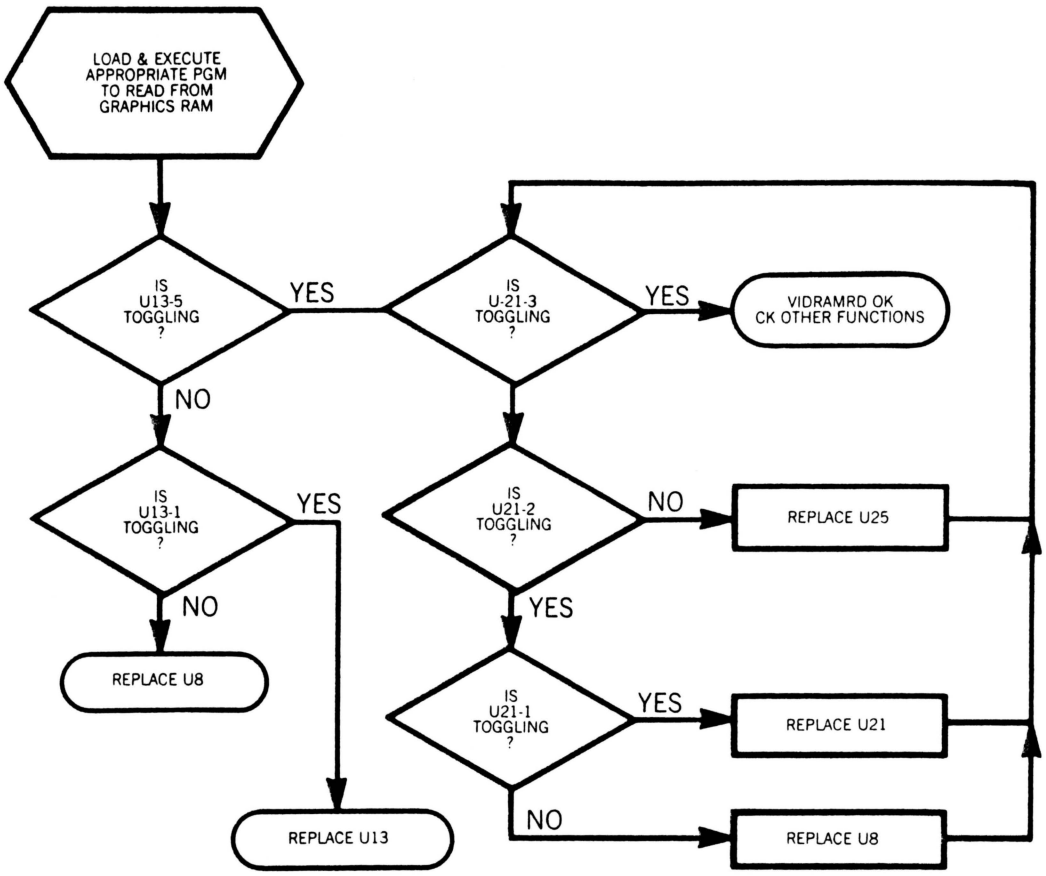
STEP 1: VERIFY BUFFERS



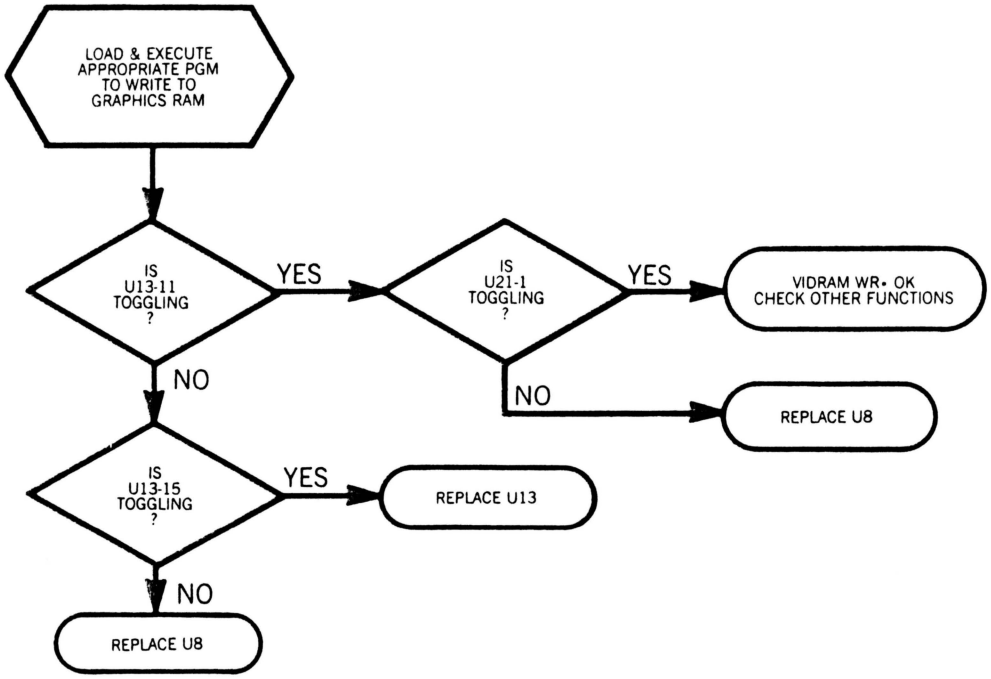
STEP 2: DECODING CHECK a. VSEL



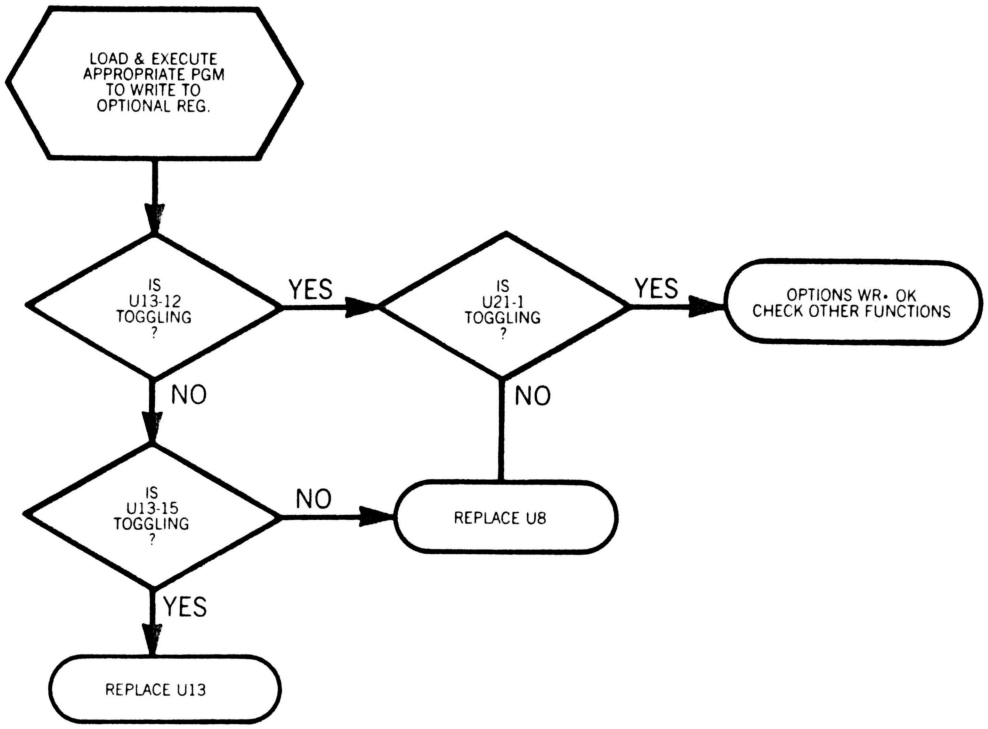
2: b. VIDRAMRD•



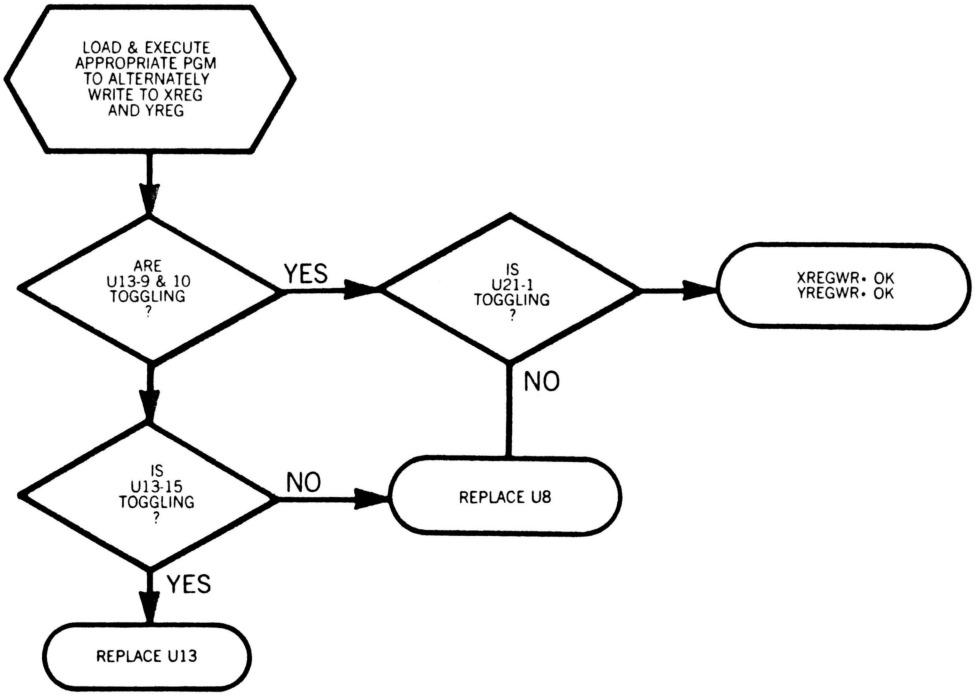
2: c. VIDRAM WR•



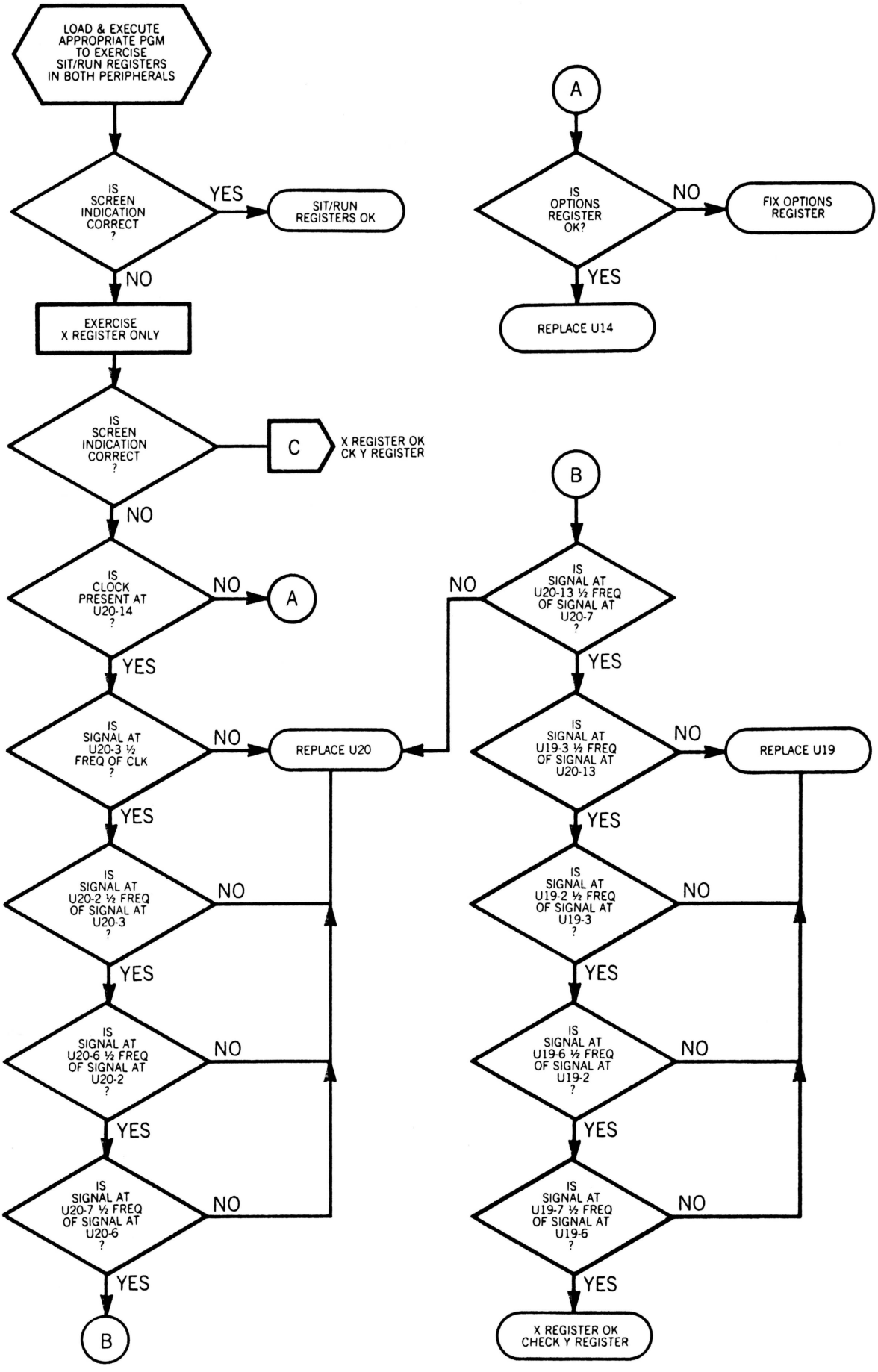
2: d. OPTIONS REGISTER WRITE CHECK



2: 3. XREGWR•, YREGWR• CHECK



Sit/Run Register Checks



Sit/Run Register Checks (continued)
(Y Register)